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by

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ABSTRACT

A concept for the visual display of the speech parameters of frequency, amplitude and duration is developed, with emphasis on the use of such a display as an aid in teaching deaf persons to speak correctly. Design criteria for a physical realization of this concept are established and discussed. The complete electronic and mechanical design and fabrication of a prototype speech parameter analyzer is described in detail. Schematic diagrams of all electronic circuitry employed and photographs of the prototype equipment are included. Preliminary performance test results are presented and discussed.

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1. Introduction.

The problem of designing an electronic system capable of displaying visible speech is one that has received considerable attention down through the years. Early systems, designed prior to the era of computer technology, utilized various rather ingenious techniques. For the most part, these tended to be somewhat dependent on mechanical innovations to accomplish the actual display.

An article in the October 1947 issue of Science Illustrated magazine describes an electronic speech translator which had just been developed by Bell Laboratories. This system employed 12 filters which activated tiny glow lamps. These lamps were arranged vertically behind a moving phosphorescent screen. In this manner, patterns were traced on the screen in real time. It is significant to this paper that patterns produced by this device were used in tests with deaf persons with limited success. The cited article lists the major shortcomings of this equipment as being its high cost and poor fidelity. In essence, the patterns produced were very complex and difficult to interpret.

Another system [17] recorded speech signals on a loop of tape. The recorded signals were then repeatedly applied to an analyzer consisting of a fixed band pass filter and a variable oscillator driven in synchronism with the tape loop. Since the oscillator frequency was different for each playback of the recorded signals, the mixing of these signals allowed different frequency components of the recorded signals to activate the output for each playback pass. The output was recorded on a drum which was also synchronized with the tape loop. The patterns thus produced were also difficult to interpret and were not produced in real time.

Several devices have utilized the cathode ray tube to display the desired patterns. Among these was one [ 14 ] that sampled the output of 12 filters and displayed the patterns on the cylindrical sidewalls of a specially constructed tube. Another [ 3 ] similarly displayed the patterns on a PPI scope. A somewhat different approach [ 7 ]

processed speech signals and displayed so called "vectorgrams" on the face of a cathode ray tube. In this display successive line segments (vectors) appeared on the screen. The length of the line segments represented amplitude, and the direction represented frequency.

More recent efforts have emphasized not so much a visual display of speech parameters, but rather have been most concerned with quantizing and digitalizing these parameters in order to make them compatible with computer processing. Typical of such systems is one developed at Stanford University [ 16 ]. The author was privileged to visit the Stanford Electronics Laboratories in January 1967 and discuss their efforts in this field with Mr. Calvin Teague and Mr. R. J. Brown. These gentlemen were kind enough to demonstrate the operation of their equipment, and provided a basic understanding of the more pertinent technical problems involved which has proved to be of great value in guiding subsequent efforts.

2. A Speech Parameter Display Concept.

A major shortcoming characteristic of early efforts to solve the problem of visual speech display seems to be that the patterns produced were very complex and difficult to interpret. It is natural that the designers felt compelled to extract the maximum possible information from the input signals, and to faithfully record this information in the display. An inevitable side effect of such efforts is the need for highly sophisticated and costly processing equipment. Another undesirable feature of the real time display equipments was that the patterns produced were transitory in nature.

All of these systems chose to concentrate on the parameters of frequency, amplitude (intensity), and time. The frequency and amplitude information was plotted as a function of time in the displays, and was sampled as a function of time in the quantizing processes.

Since the time parameter seemed to be the cause of most of the display complexities, the author sought to discover some other related parameter to display. A study of the pictorial representation of the

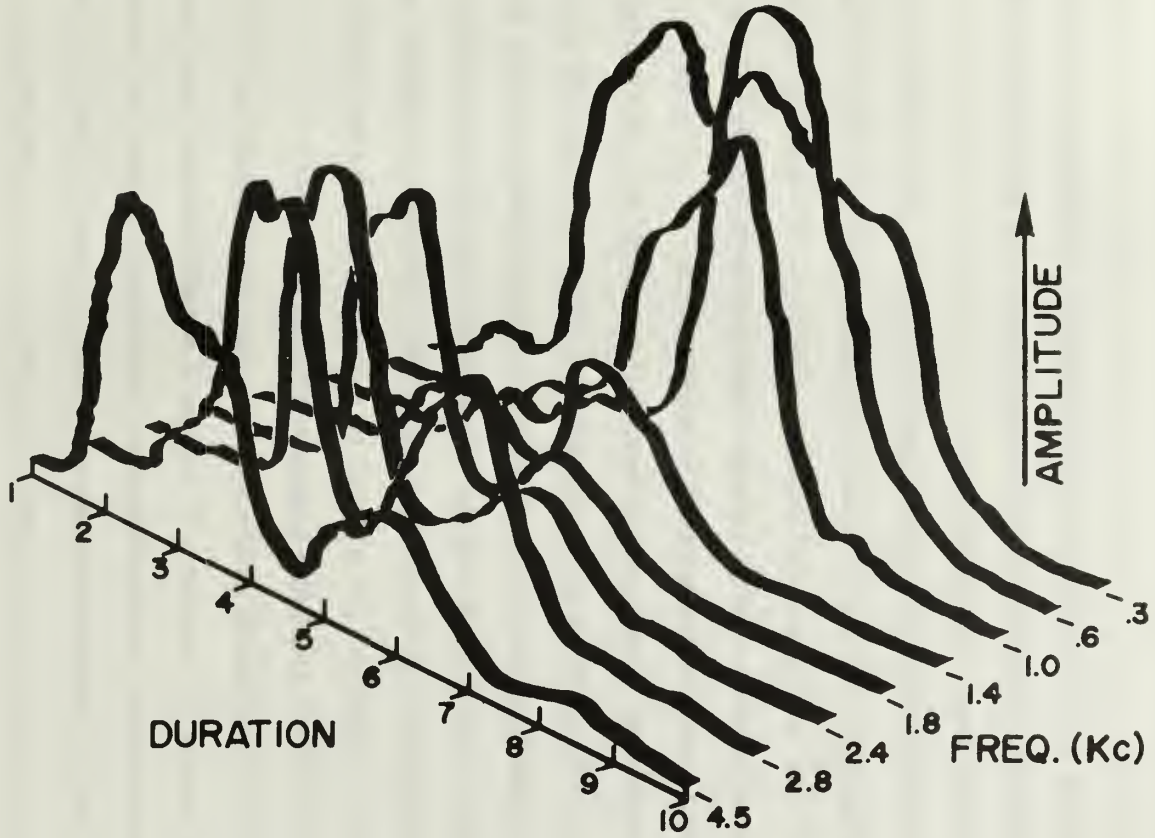


Figure 1. Spectral structure of the spoken word "ZERO".

spectral structure of the spoken word "zero" in a technical report published by the Stanford Electronics Laboratories [ 7 ] inspired the author to settle on a parameter which will be referred to as "duration". This parameter will represent a measure of the time interval during which the output of each filter exceeds some predetermined level. An adapted version of the pictorial representation cited is reproduced herein as Figure 1.

Thus, as a first element of the concept of speech parameter display, it is established that the parameters to be displayed will be frequency, amplitude, and duration.

The second element of the concept, based on the advent of computer technology, is that the chosen parameters will be entirely quantized and/or digitalized prior to display. By this means it is hoped to encompass a wide range of information with a less complex pattern which can be more readily interpreted.

The next consideration concerns the type of display to be used. The major problem here is to choose a display pattern that will be as simple as possible and still retain sufficient detail to make the pattern meaningful. This relates to the second element insofar as the separation of quantizing levels is concerned. Of major concern was the desire that, whatever the method of display, the pattern remain fixed for as long as desired after being produced.

Although it seemed evident that a bar graph would be the simplest possible pattern to display, it was not immediately evident how one might display three parameters simultaneously on one bar graph. Another prospect was some sort of a matrix representation of these parameters. Here again the problem of plotting three parameters in two dimensions was evident. The compromise, and final element of the concept, involves the utilization of a display consisting of a matrix of indicator lamps wherein the upper half of the matrix represents a bar graph of amplitude versus frequency and the lower half of the matrix produces a digital pattern representing duration versus frequency.

In summary, the concept is to quantize the speech parameters of frequency, amplitude, and duration, and to provide for a stationary and very much simplified display of the resulting information by means of a matrix of indicator lamps.

3. Design Criteria.

The objective was to design and build a prototype electronics system capable of providing a stationary visual display of the speech parameters of frequency, amplitude, and duration. All parameters are to be quantized and/or digitalized prior to display. The display will consist of a matrix of indicator lamps arranged in such a manner that the upper half of the matrix will represent a plot of amplitude versus frequency and the lower half of the matrix will indicate duration versus frequency.

Quantizing levels are to be chosen to minimize pattern complexity without detracting too much from the information content of the pattern.

Since it is intended that the prototype equipment be utilized in a project to study the feasibility of using such a device as an aid in teaching deaf persons to speak more correctly, it is mandatory that only readily available and relatively inexpensive components be utilized. Further, the equipment should be portable and simple to operate.

4. The System.

The final system design, achieved after several false starts and considerable compromise of conflicting considerations is shown in block diagram form in Figure 2.

The output of a microphone is amplified to a useable level in a preamplifier which in turn drives a bank of 10 active filters in parallel. These filters quantize the frequency spectrum over the range of 400 to 4000 hertz into 10 discrete samples. The output of each filter is taken through a buffer amplifier which was found necessary in order to prevent subsequent circuitry from unduly loading the filters.

One output from the buffer amplifier drives a four level amplitude detector which in effect quantizes the amplitude parameter of the

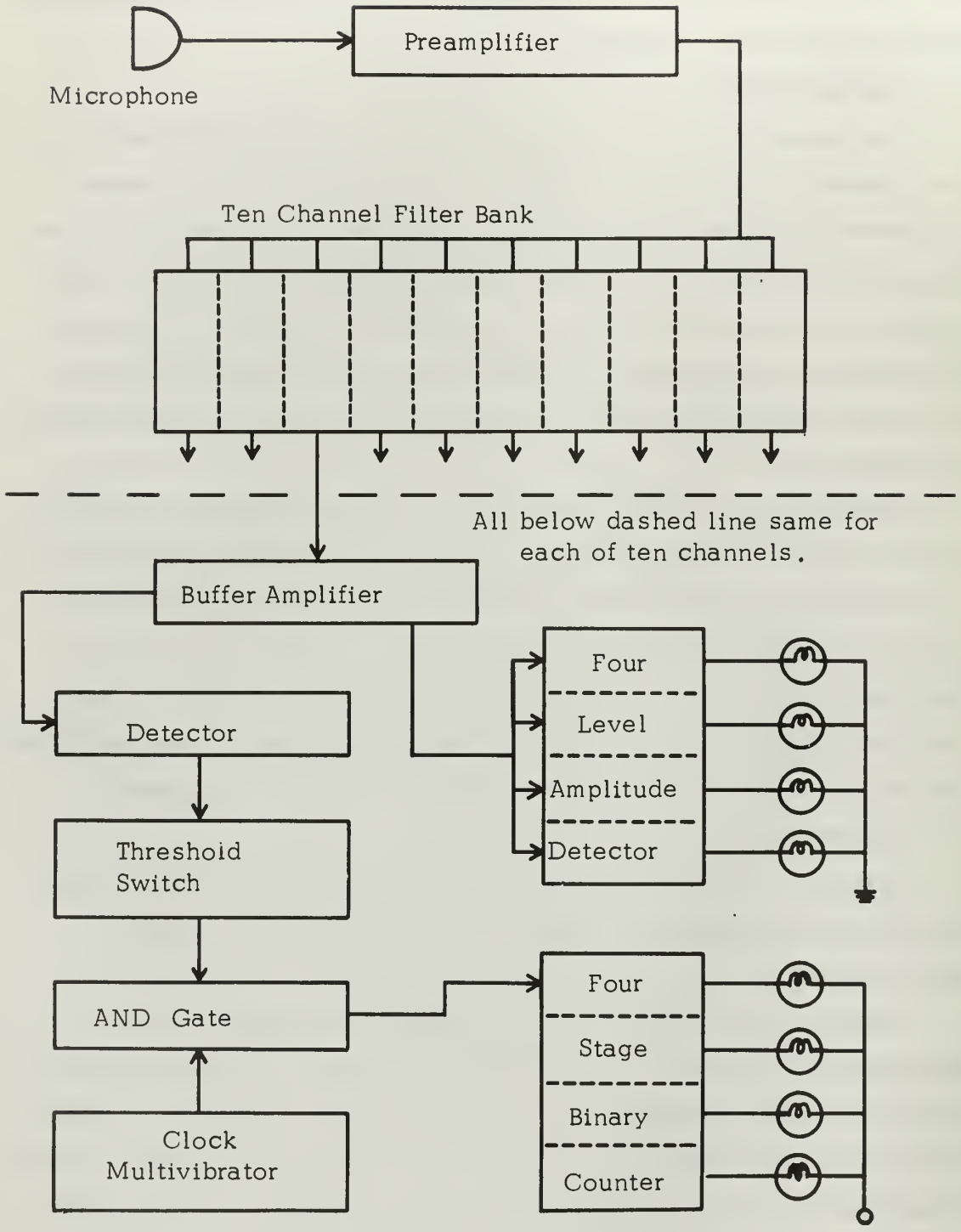


Figure 2. System Block Diagram.

signal and directly activates the four amplitude indicator lamps associated with that channel.

The other output of the buffer amplifier is processed in an envelope detector and used to excite a threshold switch. The output of the threshold switch is a binary "level" logic signal which is HI (high) when the switch is on and LO (low) when the switch is off. The logic signal provides one input to an AND gate. The other input to the AND gate is provided by a clock multivibrator which runs continuously. In this manner the clock pulses appear at the output of the AND gate only when the threshold switch is turned on by the output of the envelope detector. The clock pulses out of the AND gate energize a four stage binary counter circuit. The complementary outputs of the binary counter stages activate lamp drivers which control the four duration indicator lights for the channel.

The total display consists of a matrix of 80 indicator lamps arranged in 10 columns representing frequency quantization, and eight rows, the top four of which represent amplitude quantization and the bottom four of which represent duration quantization. Front panel controls include a preamplifier gain control, a display reset button, and two multivibrator speed controls. These latter were included in the prototype equipment only to allow for the experimental evaluation of the effect of counter speed on the duration pattern. Photographs of the prototype equipment are included in Appendix II.

5. Preamplifier Design.

Since the preamplifier must directly drive all ten of the active filters, it was decided that an operational amplifier design would best serve the purpose. Several commercially available integrated circuit operational amplifiers were considered, and the Fairchild 7709 High Performance Operational Amplifier was selected. This element was used in a simple standard feedback configuration with necessary frequency compensation as shown schematically in Figure 3. The 7709 comes in an epoxy TO-5 configuration, and the pin numbers shown in the schematic

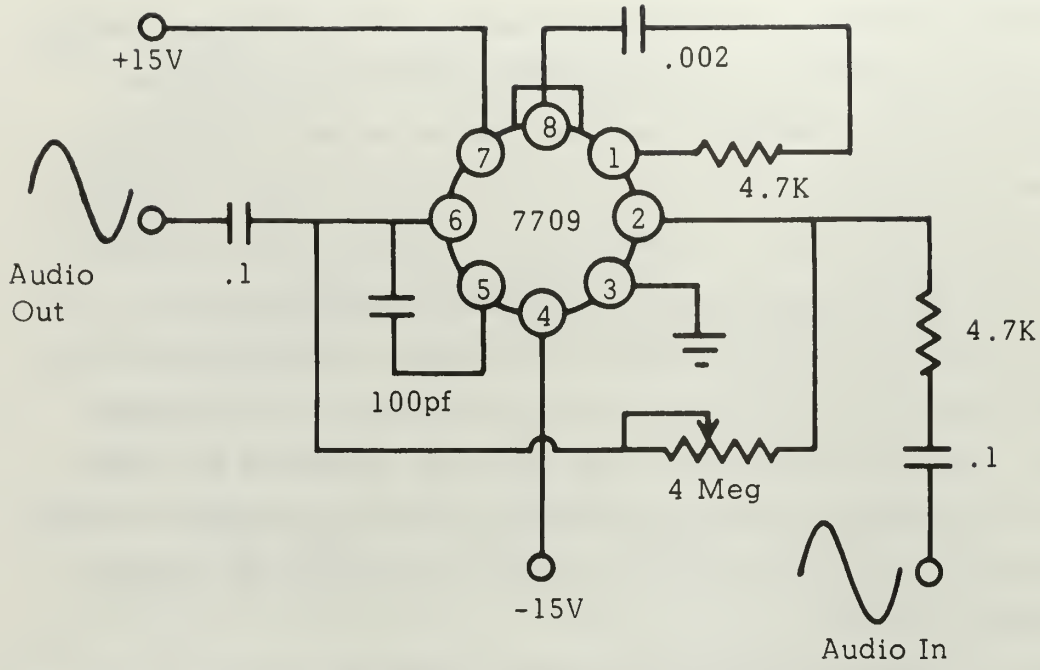


Figure 3. Microphone Preamplifier.

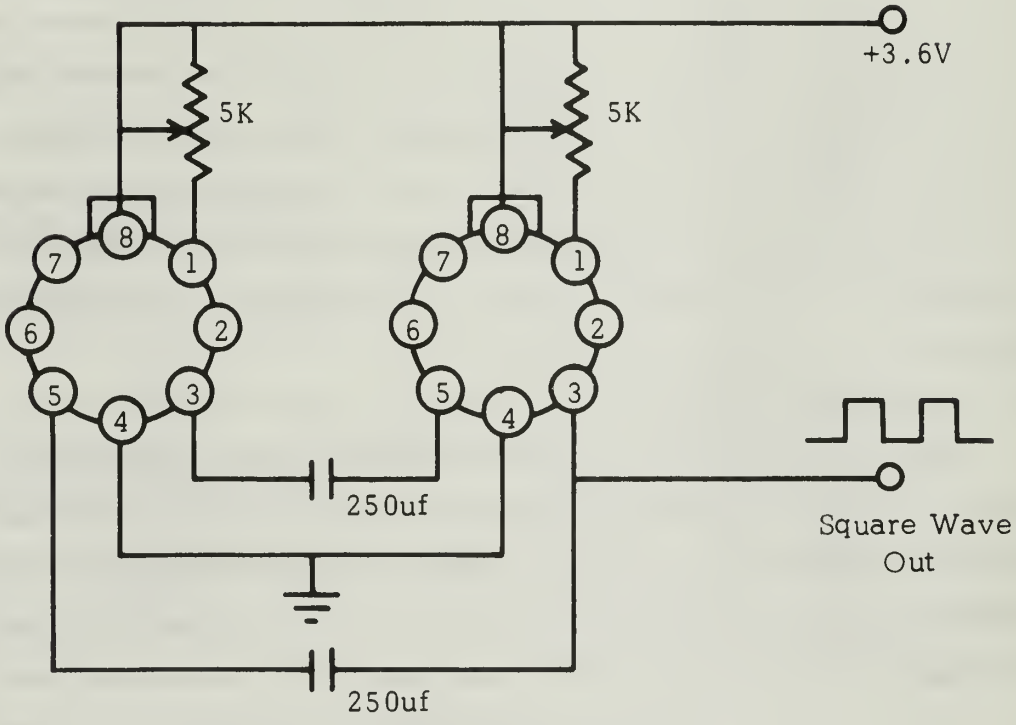


Figure 4. Clock Multivibrator.

are as seen from the bottom of the element. The detailed circuitry employed in the 7709 is shown schematically in Figure 14. Performance data for this and all other Fairchild integrated circuits employed are readily available from the manufacturer.

While the 7709 is a fairly expensive element, the need for a high gain preamplifier capable of driving ten active filters is felt to justify its use in this case.

6. Clock Multivibrator Design.

The need for compact circuitry, reliable operation, and ability to drive ten AND gates led to the utilization of another Fairchild integrated circuit package in the clock multivibrator design. Here two very inexpensive Fairchild 9900 Medium Power Buffer elements were combined in the extremely simple multivibrator circuit shown schematically in Figure 4.

This almost foolproof circuit operates very well over a wide range of frequencies and in particular at the low frequencies desired in this design. A nominal frequency of five Hertz was selected in the early design stages, but the clock frequency can be varied from two Hertz to 15 Hertz by means of the two 5k potentiometers. Two potentiometers are employed in this case to keep the square wave output symmetrical. The detailed circuitry included in the Fairchild 9900 package is shown schematically in Figure 11.

7. Active Filter Design.

This design represents a significant contribution to this project by the personnel of the Stanford Electronics Laboratories as mentioned in the introduction. Mr. R. J. Brown referred the author to a pair of handbooks distributed by the Burr-Brown Research Corporation [ 1 and 2 ] that describe the use of operational amplifiers in a multitude of configurations, including frequency selective amplifiers which are in essence active filters. Mr. Brown further provided the author with a schematic diagram of the operational amplifier circuitry shown in Figure 5.

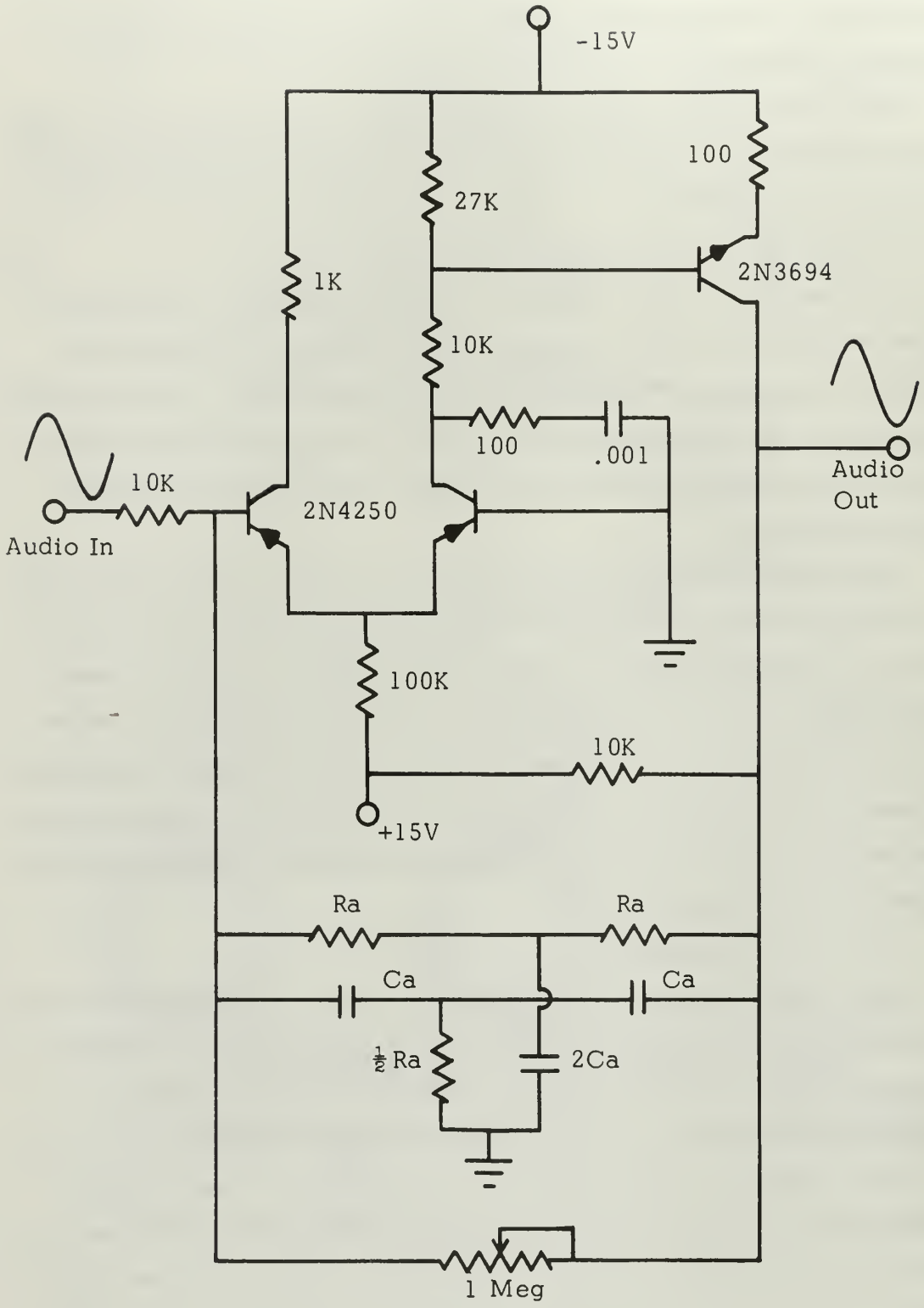


Figure 5. Active Filter.

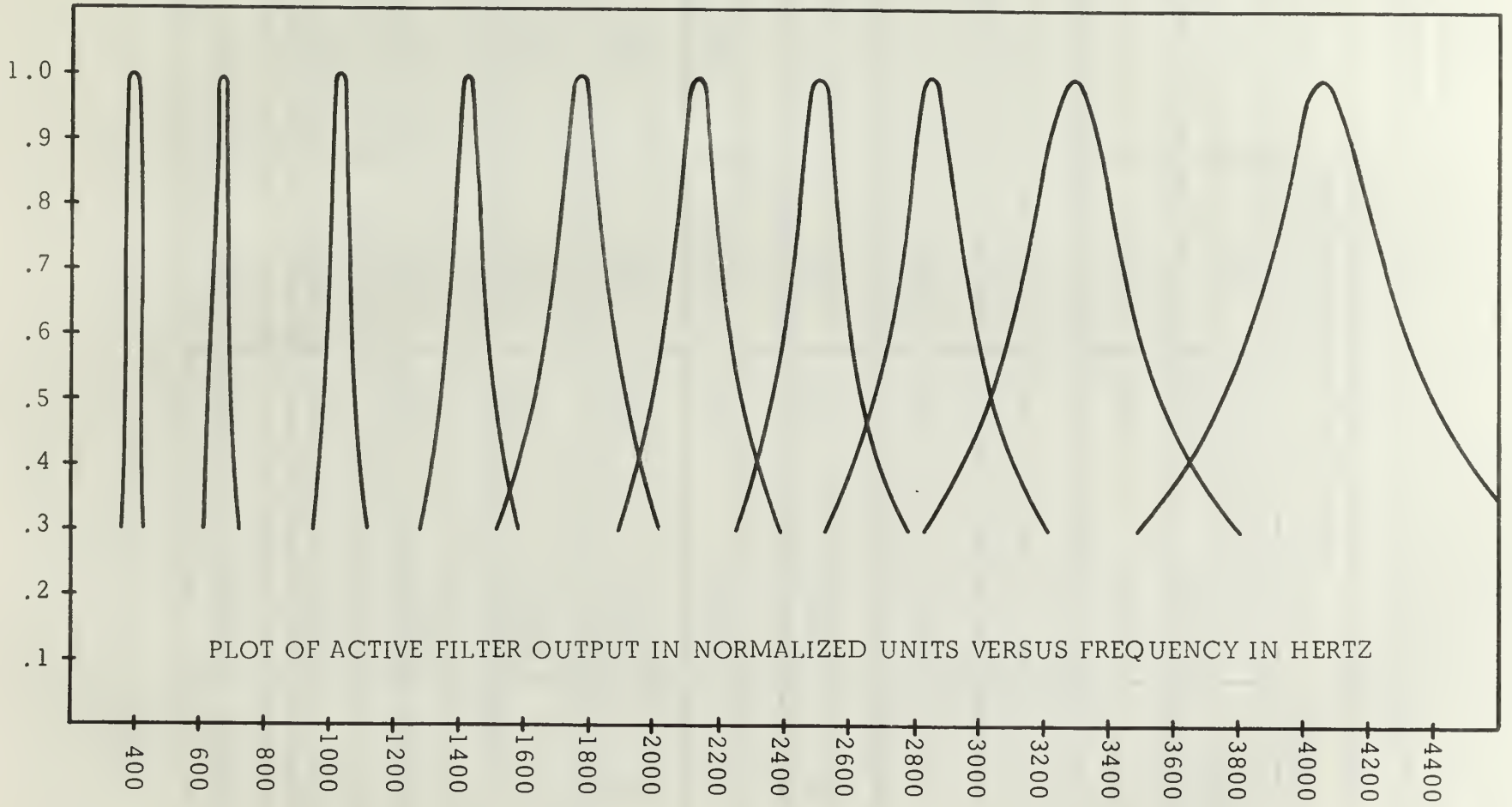


Figure 6. Normalized relative frequency response of the ten active filters. The gain of all channels is equalized at 33 db at the center frequency.

Table 1. Channel center frequencies and active filter component values.

| Channel | Center Frequency Design | Actual | Ra | Ca |
|---|---|---|---|---|
| 1 | 389 | 395 | 8.2K | .05 |
| 2 | 710 | 670 | 6.8K | .033 |
| 3 | 970 | 1030 | 8.2K | .02 |
| 4 | 1450 | 1425 | 11K | .01 |
| 5 | 1740 | 1775 | 14.2K | .0064 |
| 6 | 2185 | 2130 | 13K | .0056 |
| 7 | 2585 | 2510 | 11K | .0056 |
| 8 | 2900 | 2860 | 11K | .005 |
| 9 | 3400 | 3310 | 14.2K | .0033 |
| 10 | 3990 | 4050 | 20K | .002 |

As can be seen from the diagram, the operational amplifier employs only three inexpensive transistors which are also Fairchild products. The frequency selectivity is provided by means of a twin "T" feedback network which, in connection with the operational amplifier, provides an over-all transfer function for the circuit very much the same as that of a highly selective band-pass filter. The center or "resonant" frequency of the active filter is given by the relationship $fo = 1/2\ \pi\ RaCa$, where Ra and Ca are the elements of the twin "T" network arranged as shown in the Figure. The gain of the active filter at the center frequency can be adjusted by means of the one megohm potentiometer connected in parallel with the twin "T" feedback network. This allows one to equalize the gain of the various filters and compensate for non-uniformities in the frequency response of the overall system.

It is to be noted that the Q and hence the bandwidth of the active filters is related to the gain at the center frequency. A higher gain gives a higher Q and a narrower bandwidth to the overall filter response curve. Figure 6 shows the normalized relative frequency response curves for all ten active filters as measured on the prototype equipment.

While the bandwidth characteristics are not uniform for the various filters as included in the prototype equipment, it is felt that the frequency quantization provided is sufficiently uniform to provide for meaningful evaluations of the basic concept involved herein. Furthermore, it is anticipated that the active filter characteristics can be made more uniform by experimenting with different combinations of Ra and Ca and/or by employing more sophisticated operational amplifiers. While the latter was ruled out by the author in the design of this equipment because of high cost, recent issues of various trade journals have advertised reasonably high performance integrated circuit operational amplifiers for less than seven dollars apiece.

8. Buffer Amplifier, Detector, and Threshold Switch Design.

The original design did not include a buffer amplifier following the active filter, but preliminary tests showed that the loading effect of

subsequent circuitry changed the filter characteristics and made proper operation somewhat dependent on the individual elements in the circuit. As shown in the upper left portion of the schematic diagram of Figure 7, the buffer amplifier consists of a 2N708 transistor biased just beyond the linear region into saturation, and a 2N736A transistor employed as an emitter follower. The purpose of biasing the 2N708 into saturation is to keep the base of the 2N736A at zero potential when no signal is present. This helps to eliminate spurious activation of the amplitude detectors and provides a definite reference point for the design and adjustment of subsequent circuitry.

One output of the emitter follower is taken directly from the emitter through a 4.7K resistor to the amplitude detector circuitry which is described in detail in Section 10. The other output is taken from a simple envelope detector included in the emitter circuit. The 10K resistor across the 35 microfarad capacitor of the detector is chosen so as to slightly emphasize the envelope duration in order to allow more counts to be registered on the binary counter for inputs of very short duration.

The slowed-down envelope signal from the detector is coupled through a 12K resistor to the threshold switch circuitry shown in the lower half of Figure 7. The threshold switch is a modified Schmitt trigger. The right hand transistor is normally cut off and the left hand transistor is normally in saturation. In this state the "level" output signal, taken from a voltage divider across the saturated transistor, is at a zero voltage or LO level. When an input signal causes the detector output to rise above a pre-determined level, adjusted to be just below the level needed to activate the first amplitude indicator lamp, the right hand transistor switches on and the left hand transistor switches off. The "level" output then rises to a HI level of approximately 1.3 volts. When the output of the envelope detector drops below the pre-determined level the action reverses and the "level" output again drops to LO.

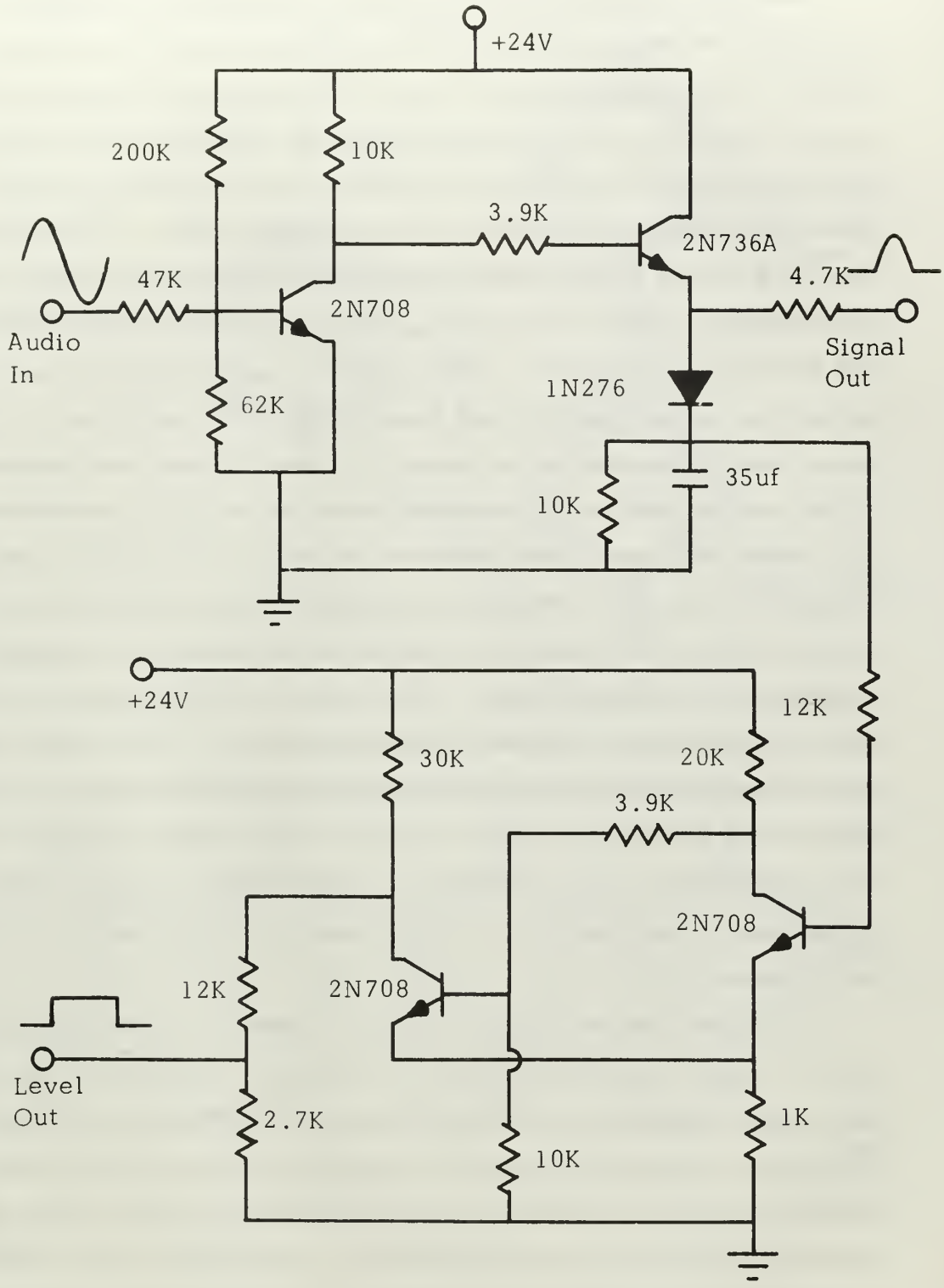


Figure 7. Buffer Amplifier, Detector, and Threshold Switch.

9. Duration Counter Design.

Here again extensive use of Fairchild integrated circuits greatly simplifies the design problem and contributes a great deal to cost reduction. As shown in Figure 8, the clock multivibrator output and the "level" output from the threshold switch are separately led through individual Fairchild 9900 Buffer-Inverters to two of the four available inputs of a Fairchild 9914 Dual Two Input NAND Gate. In this manner, the clock pulses appear at the corresponding output of the NAND gate only when the "level" input is HI. One half of the dual NAND gate is not utilized in this design. This somewhat wasteful practice is justified by the low cost of the 9914 and because the use of individual printed circuit plug-in boards for the circuitry of each channel as described in a later section makes the dual employment of one 9914 impractical.

Since the clock pulses appear at the output of the NAND gate only during that time when the input is exceeding some specified level, this output contains the necessary information to measure the quantized duration of the channel output. This signal is then applied to the input of a four stage binary counter as shown in Figure 9. The counter consists of four Fairchild 9923 JK Flip Flop integrated circuits. The state of each flip flop is indicated by a lamp in the duration section of the display matrix. Hence, the duration display can count up to 15 discrete segments of duration at any rate that can be set on the clock multivibrator.

The actual activation of the duration lamps is by means of lamp drivers in the configuration shown in Figure 10. The 2N3417 transistor is normally saturated in this circuit and is cut off when the 2N3394 transistor is turned on by a HI level signal from one of the JK flip flops. For this reason, the indicator lamp is on when the input to the lamp driver is LO and off when the input is HI. While this is the opposite to what one might expect, the inequity is solved by using the complementary output of the JK flip flop to activate the lamp driver. The overall effect is then to have the lamps count for a HI "level" input

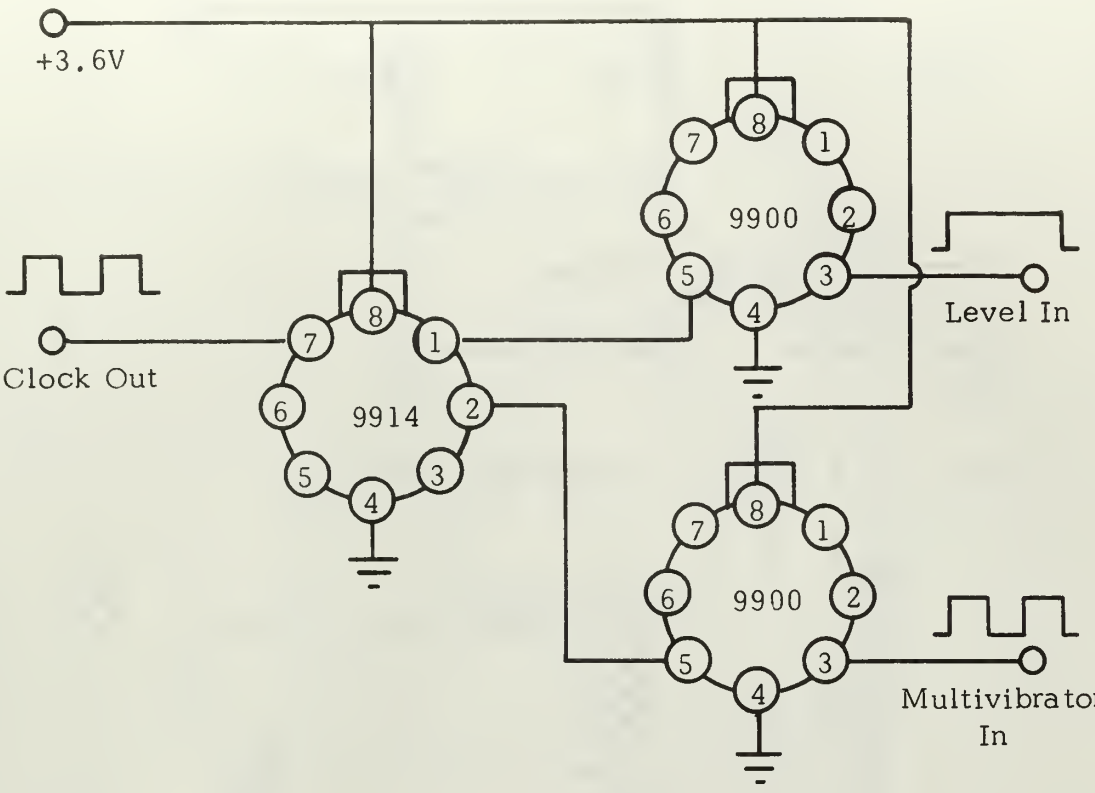


Figure 8. AND Gate.

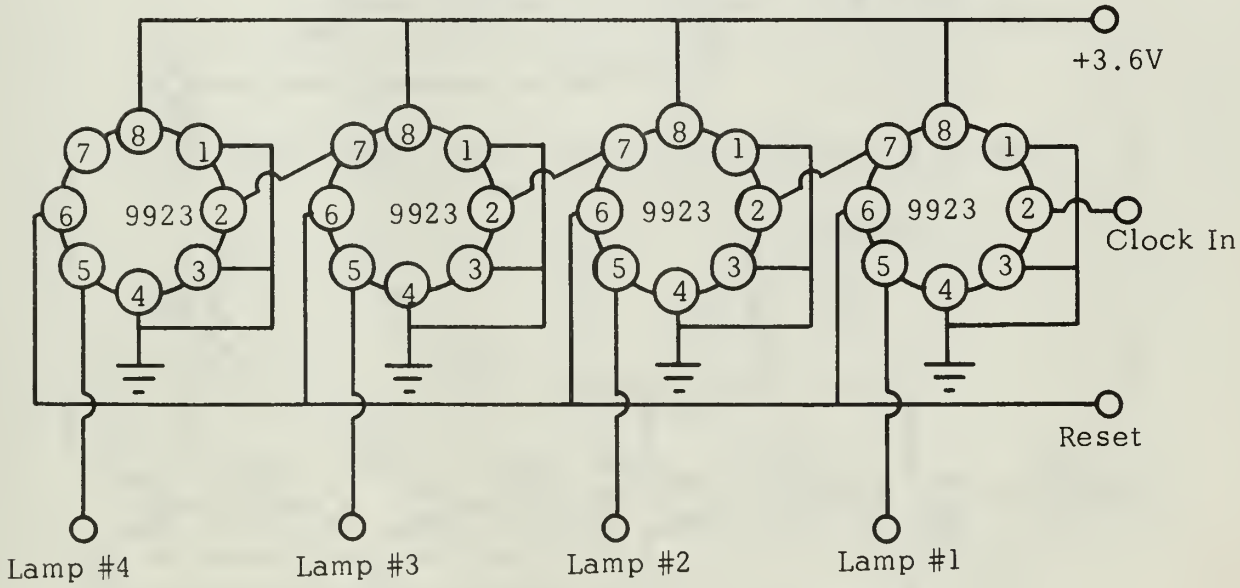


Figure 9. Four Stage Binary Counter.

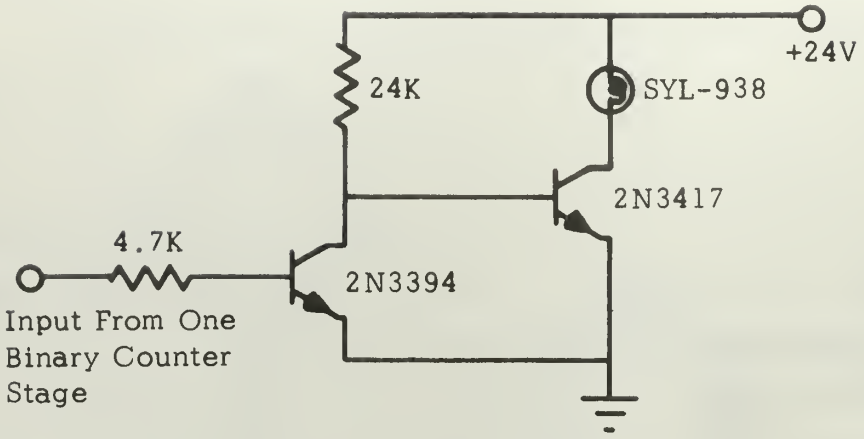


Figure 10. Duration Counter Lamp Driver.

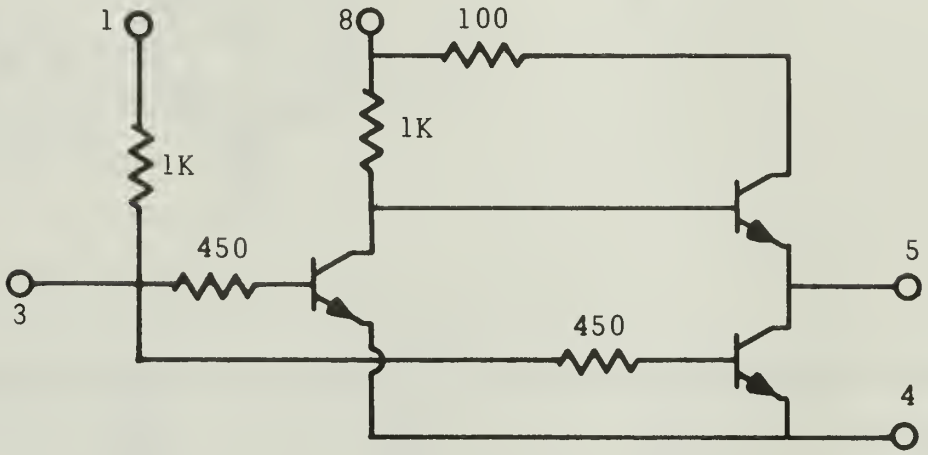


Figure 11. Fairchild 9900 Medium Power Buffer Detail.

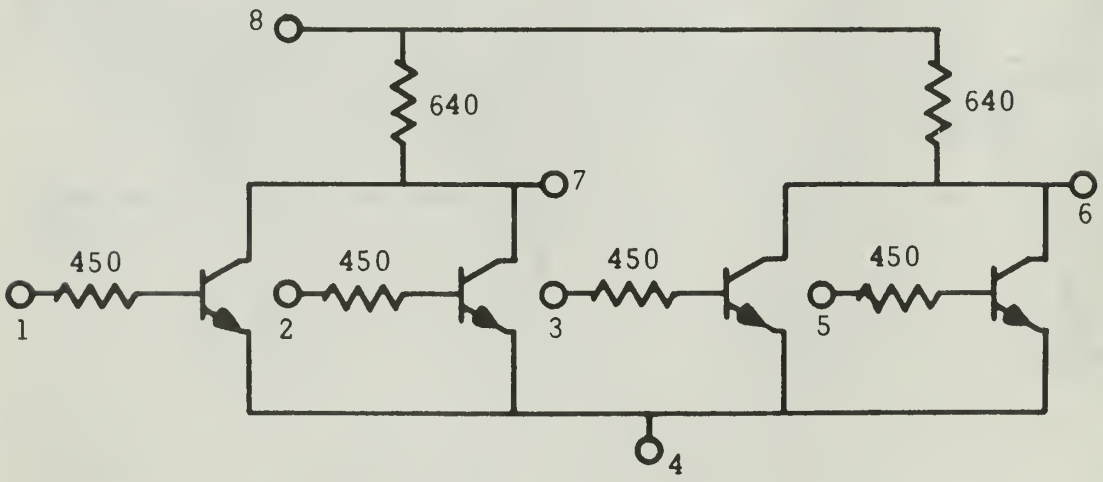


Figure 12. Fairchild 9914 Dual Two Input Gate Detail.

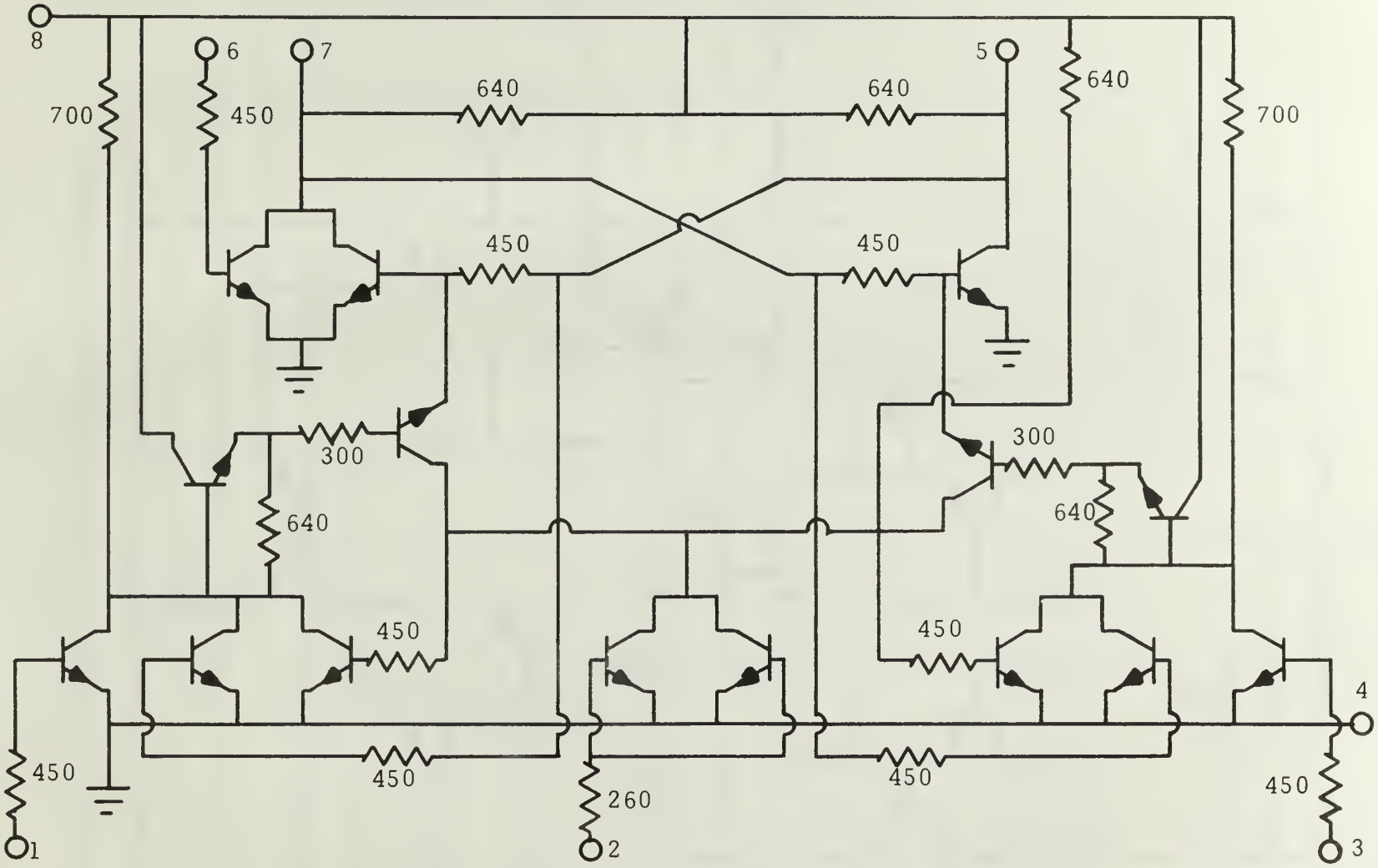


Figure 13. Fairchild 9923 Medium Power JK Flip Flop Detail.

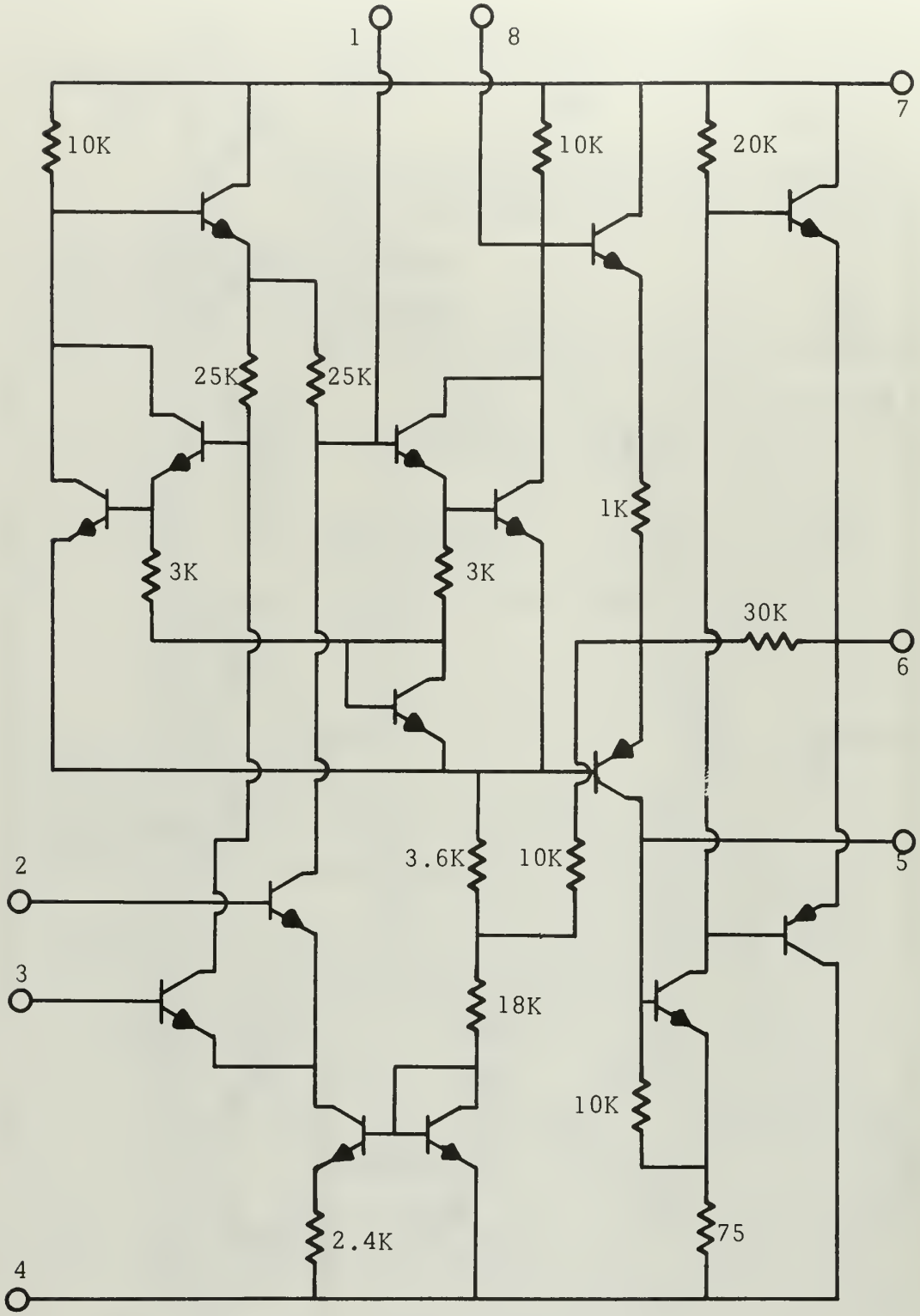


Figure 14. Fairchild 7709 High Performance Operational Amplifier Detail.

coincident with HI clock states and to have all lights go out when the reset input to the JK flip flops is activated. This is as it should be.

The pin numbering on the schematic diagrams of all Fairchild integrated circuits discussed in this section are as seen from the bottom. The details of the 9914 Gate and the 9923 JK Flip Flop are as shown in Figure 12 and Figure 13 respectively.

10. Amplitude Level Detector Design.

This circuitry proved to be the most difficult to design, and has subsequently presented many problems of erratic operation and performance. The basic difficulty lies in the requirement that once an amplitude indicator lamp is turned on it must remain on until manually reset, regardless of the nature of the input signal. This consideration, along with the requirement to keep the cost down, led to the utilization of 3N84 silicon controlled switches as lamp drivers. The 3N84 is easy to turn on, reacts very quickly, and can easily handle the indicator lamp current. The most persistent problem encountered in the early design stages was that transients created by one 3N84 switching on activated one or more of the other 3N84's thereby creating a chain reaction which continued until all had fired. Furthermore, since the lamps are in the cathode circuit of the silicon controlled switches, the cathode gate rises to plus 24 volts when the switch fires. This sharp rise was coupled to the inputs of the other switches and compounded the chain reaction problem. As if all this was not enough, it was discovered that the firing point of various 3N84's was significantly different. In other words, different 3N84's installed in the same circuit would fire at different levels.

With this background in mind, one can proceed with an explanation of the operation of the circuitry shown schematically in Figure 15. The input signal, taken through a 4.7K resistor directly from the emitter follower of the active filter buffer amplifier, is applied to a voltage divider consisting of a ladder network of resistors. Each of four taps on the voltage divider is led to the base of an emitter follower which is

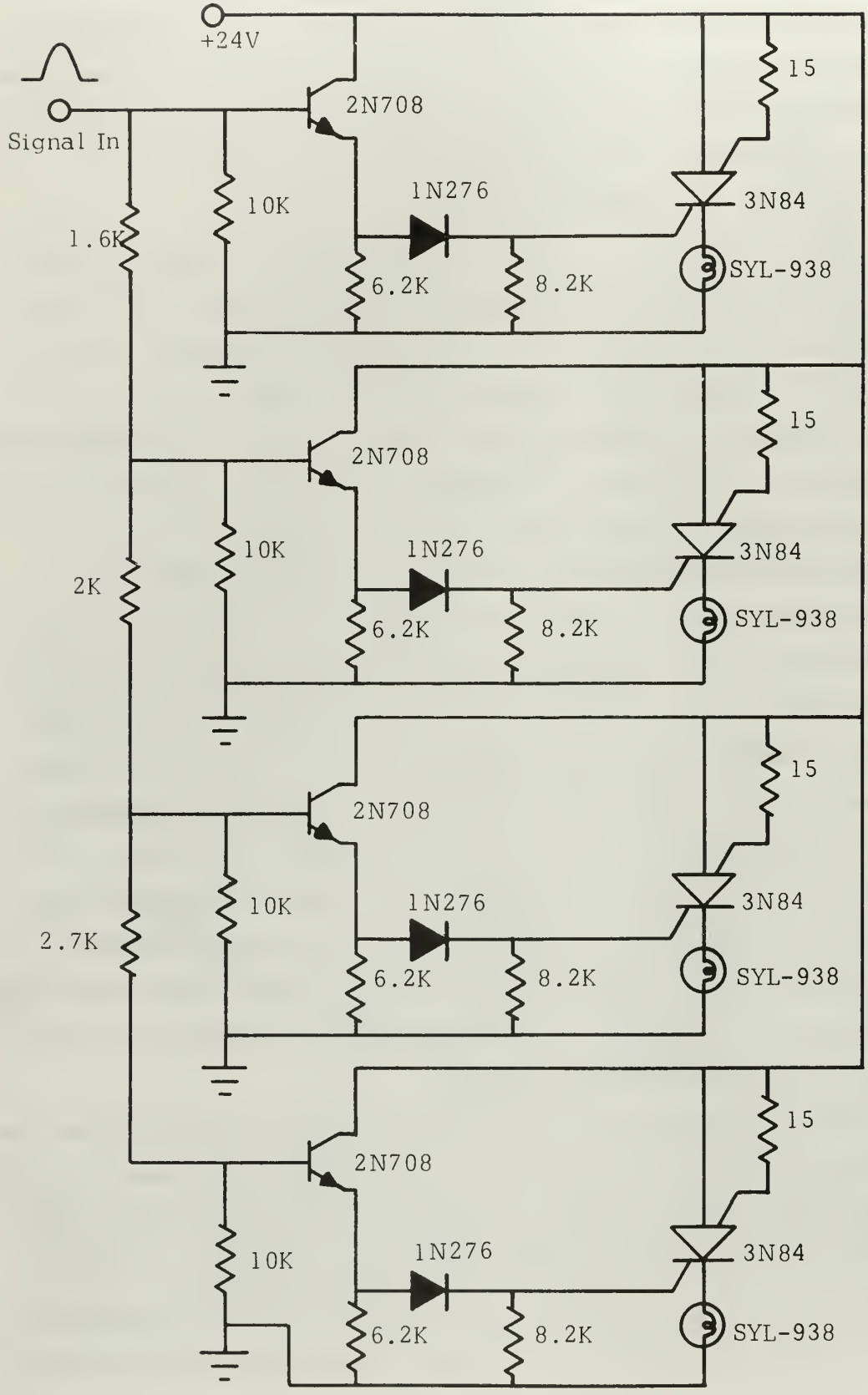


Figure 15. Four Level Amplitude Detector.

normally biased into cutoff. The emitter follower provides isolation between the ladder network, which is common to all four switches, and the input to the one silicon controlled switch in question. In the absence of an input signal the emitter is at ground potential. The 1N276 diode is back biased whenever the switch fires and the plus 24 volt level appears on the cathode gate. This effectively disconnects each switch from the input circuit as it fires. The 8.2K resistor in the cathode gate circuit and the 15 ohm resistor in the anode gate circuit combine to stabilize the firing point independent of the particular device installed. The anode gate resistor serves the further purpose of helping to eliminate rate effect firing of the switches.

The switches were originally reset by opening the cathode circuit on the ground side of the indicator lamps. When interaction between the various channels proved this approach infeasible, the design was changed so as to accomplish reset by opening the plus 24 volt supply lead. Switch transients were eliminated by connecting a one microfarad capacitor across the switch contacts.

While the amplitude detector circuitry operates satisfactorily, it is considered by the author to be the least reliable section of the overall equipment, and its redesign should be considered prior to any attempt to construct additional equipments. It is not considered likely that the present configuration will detract in any way from results of anticipated evaluation projects.

11. Printed Circuit Board Design and Fabrication.

The fact that this design concept involves the use of ten sets of almost identical circuitry makes the use of printed circuit boards particularly desirable. While it was first intended that all the circuitry for one channel be incorporated onto one printed circuit card, it was subsequently decided that a more flexible and versatile system would result from the grouping of functionally related circuitry into two parts and employing two cards for each channel. Thus, as shown in Figure 16, the active filter, buffer amplifier, detector, and threshold

switch was included on one card, and, as shown in Figure 17, the amplitude detector, AND gate, binary counter, and duration lamp drivers were included on a second card. The filter card is five inches high by six inches wide, and the processing card is six inches square. These cards are designed to plug into standard 18 pin connectors in order that they might be easily removed and exchanged for ease in maintenance and trouble shooting. The microphone preamplifier and clock multivibrator circuitry, which is common to all channels, was incorporated onto a separate card as shown in Figure 18. This card is three inches high by six inches wide and also plugs into a standard 18 pin connector. The arrangement of components on these cards and the arrangement of the cards in the prototype equipment can best be understood by referring to the photographs in Appendix II.

The design and fabrication of the printed circuit cards presented something of a challenge to the author. While the source of considerable frustration at times, it is felt that the knowledge and experience gained from this effort is of considerable significance. The first attempt to produce a set of two boards manually by the tape resist method were failures. Although the tape was painstakingly applied, it was not properly pressed down, and the etching solution got under the tape in places and cut through the conducting paths. Subsequently, the preamplifier board and a set of one filter card and one processor card were successfully fabricated using the tape resist method.

Since the tape resist method was too time consuming for the production of the large number of boards required, it was decided to use the photo resist method in the fabrication of the remaining cards. A master was prepared for the filter card and for the processor card by drawing the pattern with india ink on plain white bond paper. These masters were then processed in the photo lab and a one to one sized negative prepared for each. The negatives were used to expose photo sensitive copper clad material which was then etched in the normal manner to produce the final product. Two each of the filter cards and

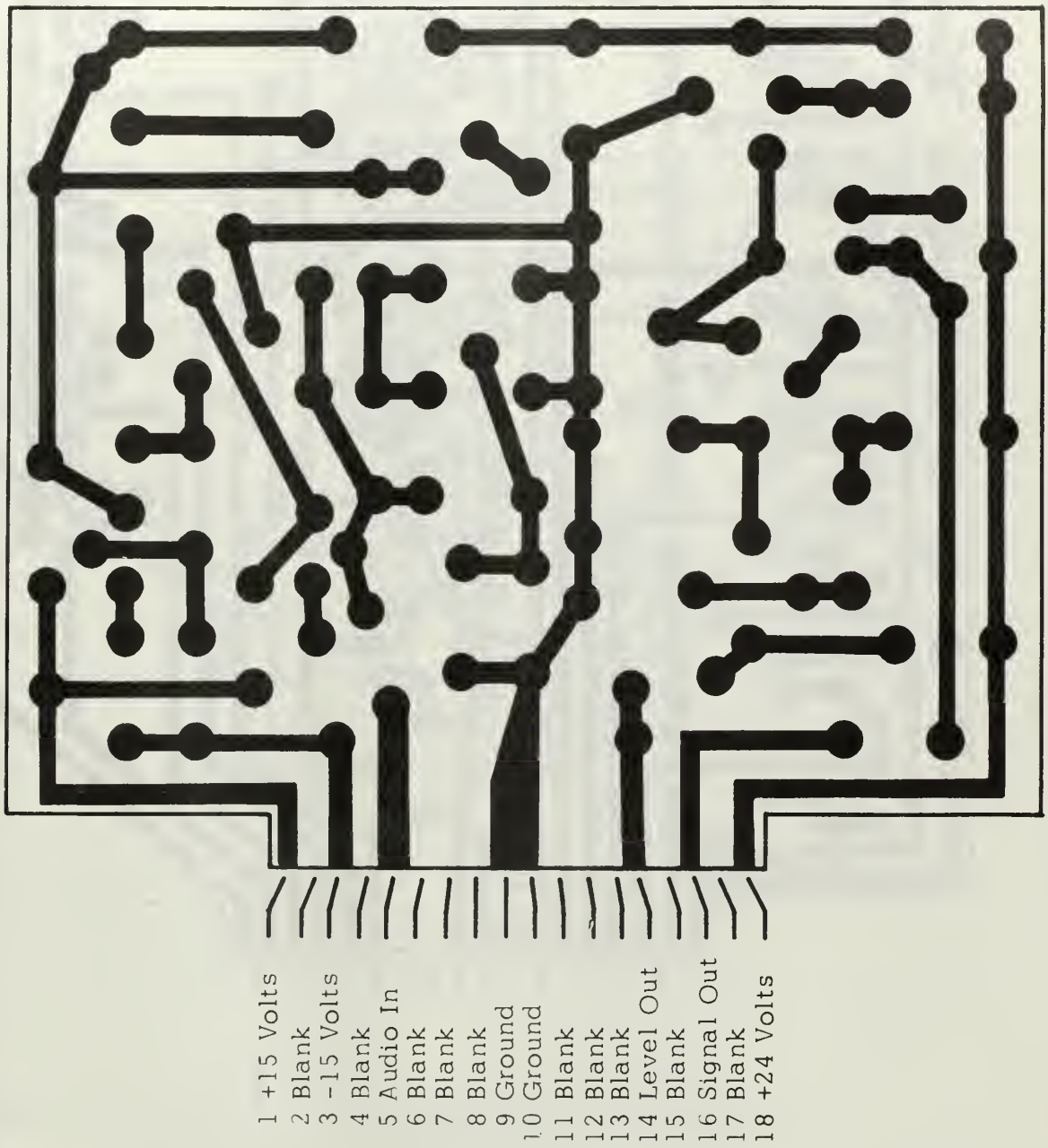


Figure 16. Filter Card. Contains active filter on the left, and buffer amplifier, detector, and threshold switch on the right. View is from copper side of board.

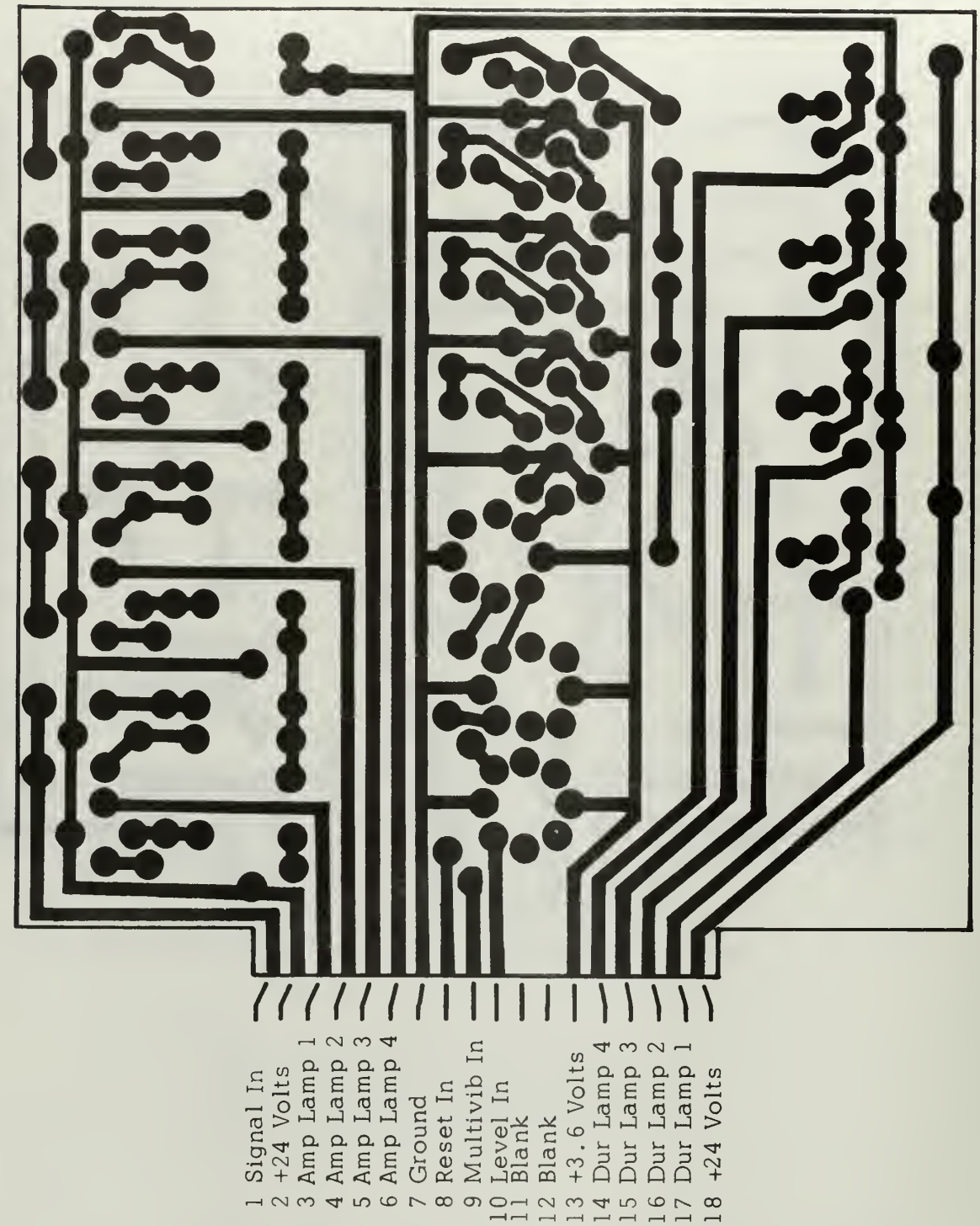


Figure 17. Processing Card. Contains four level amplitude detector on the left; buffers, AND gate and four stage binary counter in the center; and duration lamp drivers on the right. View is from the copper side of board.

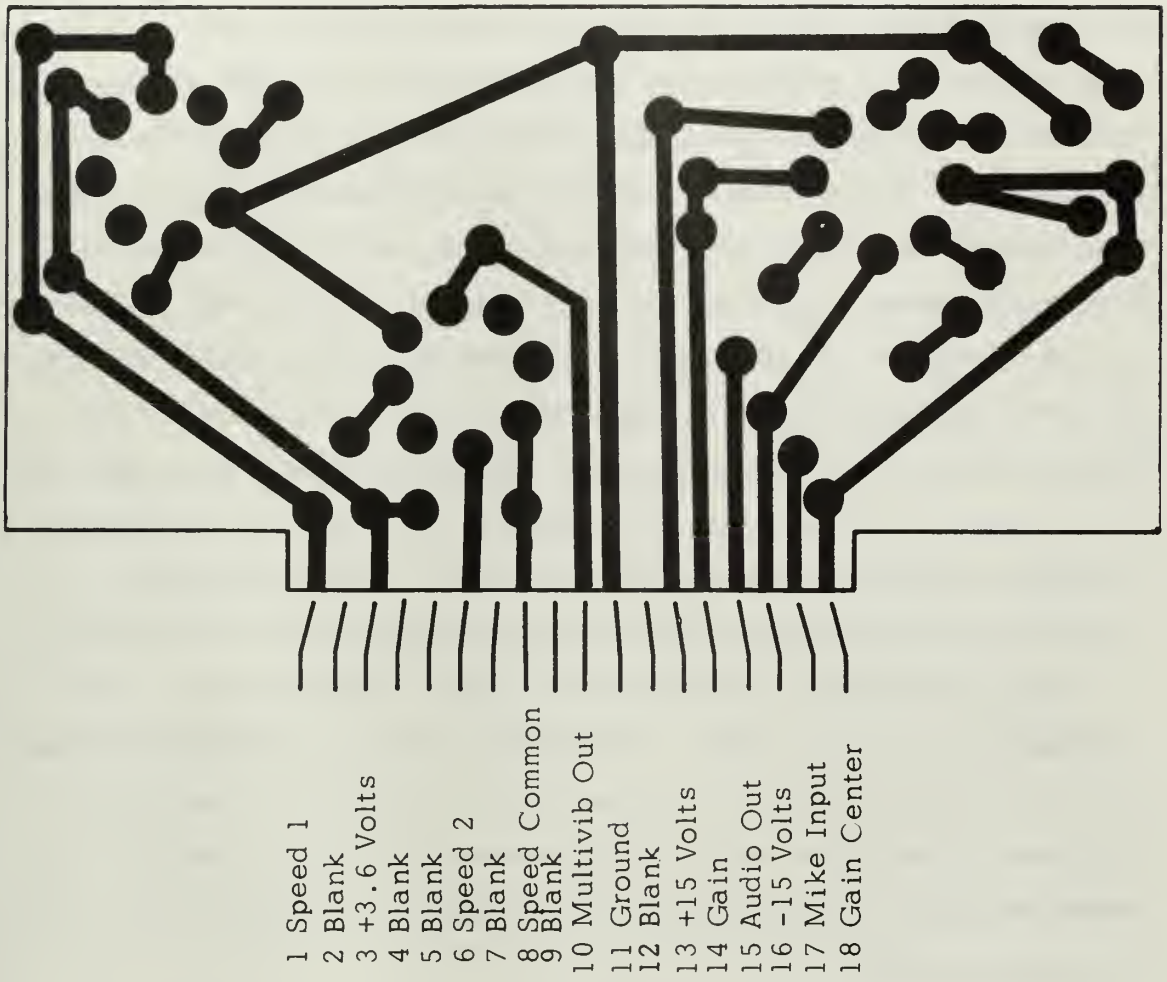


Figure 18. Preamplifier Card. Contains preamplifier on the right and multivibrator on the left. View is from copper side of board.

processor cards were fabricated in this manner. Further efforts were stymied by lack of photo sensitive copper clad material. The necessary material for this purpose had been ordered well in advance of the actual need, and has not been received to date.

For this reason it was necessary to have the remaining cards fabricated by a local commercial concern. The author worked with personnel of the commercial concern throughout the fabrication process in order to gain experience in the processing methods employed. Silk screen masters were prepared from the negatives previously used in the photo resist process. A liquid resist material was screened onto blank copper clad material and, after being allowed to dry, these were etched in a standard solution. All contact fingers were then gold plated in order to provide for better contact and higher resistance to wear and corrosion. After the cards had been drilled and routed to the proper shape, all passive components were mounted by the author. Active elements were not mounted at this time because there was some question concerning the effect of the dip soldering process on the Fairchild integrated circuits. It is believed that these elements can be dip soldered without any harm, but since no spares were available it was decided not to risk damage to those in hand. Plastic sheets were hermetically sealed over the mounted elements, and the excess wire leads of components clipped flush with the boards. All cards were then dip soldered. The author subsequently mounted the active elements by hand and the cards were ready for use.

The process described produced very satisfactory results, but seems rather involved for the fabrication of a limited number of printed circuit cards. For example, it took longer to mount the passive elements, apply the plastic protective cover, and then dip solder than it would have taken to simply mount and hand solder those same elements. The added bonus of having all copper conductors coated with solder in the dipping process is, however, significant in preventing oxidation. It is therefore suggested that if any additional equipments are to be

constructed, the cards should be dip soldered prior to drilling and all components hand soldered in place. It is felt that this will produce cards of equal quality in less time and at lower cost.

12. Power Supply Design.

The power supply requirements of this equipment are rather high due to the large number of elements employed. Each indicator lamp draws 40 milliamps of current and since there are 80 such lamps in the display the power drain on the 24 volt supply is in excess of three amperes. The hybrid combination of integrated circuits and standard elements creates a further requirement for a plus 15 and minus 15 volt supply in addition to the need for a plus 3.6 volt supply to power the logic circuitry. The plus and minus 15 volt supply drain is low since only the operational amplifiers are involved. However, the integrated logic elements each draw in the neighborhood of 15 milliamperes thereby creating a total drain in excess of one ampere for the 72 such elements employed.

With a view toward possible future expansion of the equipment to include more indicator lamps and/or more logic circuitry, it was decided to specify power supply requirements at roughly twice that actually required. It was felt that the slightly increased initial cost would be more than offset if expansion were to require the acquisition of additional power supplies. Because of the experimental nature of this endeavor and with regard to the high costs involved in any power supply combination capable of meeting the specifications imposed, it was further decided to employ commercially available modular power supplies in the prototype equipment. In this manner, the power supplies could be used to advantage in other projects or in the laboratory should such a course of action become desirable in the future. Modules selected and their specifications are as follows:

| | |
|---|---|
| 24 Volt Supply. | Universal Electronics Model M24-5.<br>Input 105-125 volts a.c.<br>Output 24 volts d.c. at 5 amps. |

| | |
|---|---|
| 3.6 Volt Supply. | Power/Mate Corporation Model RA4-3.0<br>Input 105-125 volts a.c.<br>Output 3-5 volts d.c. at 3 amps. |
| Dual 15 Volt Supply. | Powertran Model MM-15.<br>Input 105-130 volts a.c.<br>Output 15 volts d.c. at 55 milliamps |

These power supply modules are combined on one chassis as shown in the photograph in Appendix II. All supplies are brought out to the front panel for ease in measurement and for auxiliary purposes. The connection to the main chassis is through a terminal block at the rear of the power supply chassis. The wiring diagram of the power supply chassis is shown schematically in Appendix I.

NOTE: Detailed circuitry of the power supplies is available with the prototype equipment. They were not reproduced herein because proprietary information is involved.

13. Mechanical Fabrication.

The major consideration involved in the physical construction of the prototype equipment were those of portability, low cost, and flexibility. In addition, everything had to be built around the display panel, and only readily available materials employed.

Several configurations were considered and a standard relay rack type of mounting was selected. The resulting prototype equipment is best seen by consulting the photographs in Appendix II. The basic frame is a light-weight standard relay rack. The main panel is a 17½ inch by 19½ inch standard blank panel. The main chassis is a 17 inch by 13 inch by 3 inch stock model and is attached to the main panel by means of standard angle brackets. All of the printed circuit cards plug into sockets from the top of the main chassis, with the processor cards located to the front and the filter cards located directly behind them. The preamplifier card is located to the front and far right of the main chassis as viewed from the rear. This card is not visible in any of the photographs in Appendix II, but the preamplifier socket location is shown in the upper right hand corner of the main chassis bottom view. Also visible in this view are the six bus bars employed to reduce chassis wiring complexity.

The power supply front panel is a standard 5½ inch by 19 inch relay rack blank. All three power supply modules are mounted on a half chassis secured to the rear of the front panel. The potentiometer visible in the photograph of the power supply in Appendix II provides for adjustment of the 3.6 volt supply voltage. The 24 volt supply can be adjusted over a limited range by means of a screwdriver adjustment near the connector terminals on the power supply proper. No adjustment is provided for the dual 15 volt supply.

14. Preliminary Performance Test Results.

The completely assembled prototype equipment was subjected to a variety of tests, in the laboratory by the author, and at the Monterey Institute for Speech and Hearing, 969 Pacific Street, Monterey, California, by the Director, Dr. Gene England and the Director of Research, Dr. Burl Gray.

The first laboratory tests consisted of measuring the individual channel frequency response characteristics, which are depicted in Figure 6. In accordance with design criteria the channel center frequencies are evenly spaced throughout the frequency spectrum from 400 to 4000 Hertz. Also, as anticipated, the bandwidth of the channel filters increases with frequency.

Channel overlap was tested by introducing pure single frequency tones into the microphone by means of a loud-speaker connected to the output of an audio signal generator. In this manner all components including the microphone were tested. Results indicated a very good discrimination between adjacent channels and a reasonably good discrimination against harmonics so long as the gain of the preamplifier was maintained at a low enough level. Overdriving the preamplifier causes several channels to be activated by any one frequency. This effect was most apparent in the upper frequency region.

Display pattern repetition was tested by first recording the word "ZERO" on a high quality tape recorder and then noting the pattern produced by repeated replays of the recording. For a typical run of

eight patterns produced in this manner, five were found to be identical, two differed by one duration lamp and one differed by one duration and one amplitude lamp. The pattern that repeated five out of eight times is shown at the upper left in Figure 19.

The same procedure was used to determine if different sounds produced distinctly different patterns. Figure 19 shows the results for the five vowels a,e,i,o, and u. As may be seen from the figure, the patterns are distinct. By experimenting, one soon learns which sounds will activate any given portion of the display.

Tests conducted at the speech and hearing institute were from the operator and clinical application point of view. Dr. Gray indicated that he considered the concept to be good and that the prototype equipment type of matrix display held promise for clinical application. He was kind enough to offer several suggestions in connection with possible modifications to improve the utility of the equipment in a clinical application.

In this regard, it was felt that the present configuration was too sensitive to a variable input. In other words, the equipment will produce different patterns if the speaker changes the distance of the microphone from his lips or if he does not repeat the sound in exactly the same way. It was also felt that the binary duration indication was too distracting, particularly to anyone not familiar with the binary number system. Finally, it was suggested that perhaps too much information was being included in the present configuration of the display matrix. In this regard the general consensus was that while the author had taken a giant stride in the direction of eliminating extraneous information from the display it might be feasible to eliminate even more information and still retain a useable display.

15. Conclusions.

The preliminary performance test results indicate that all design criteria as originally specified are met by the prototype equipment. The evaluation of this equipment by persons experienced in speech

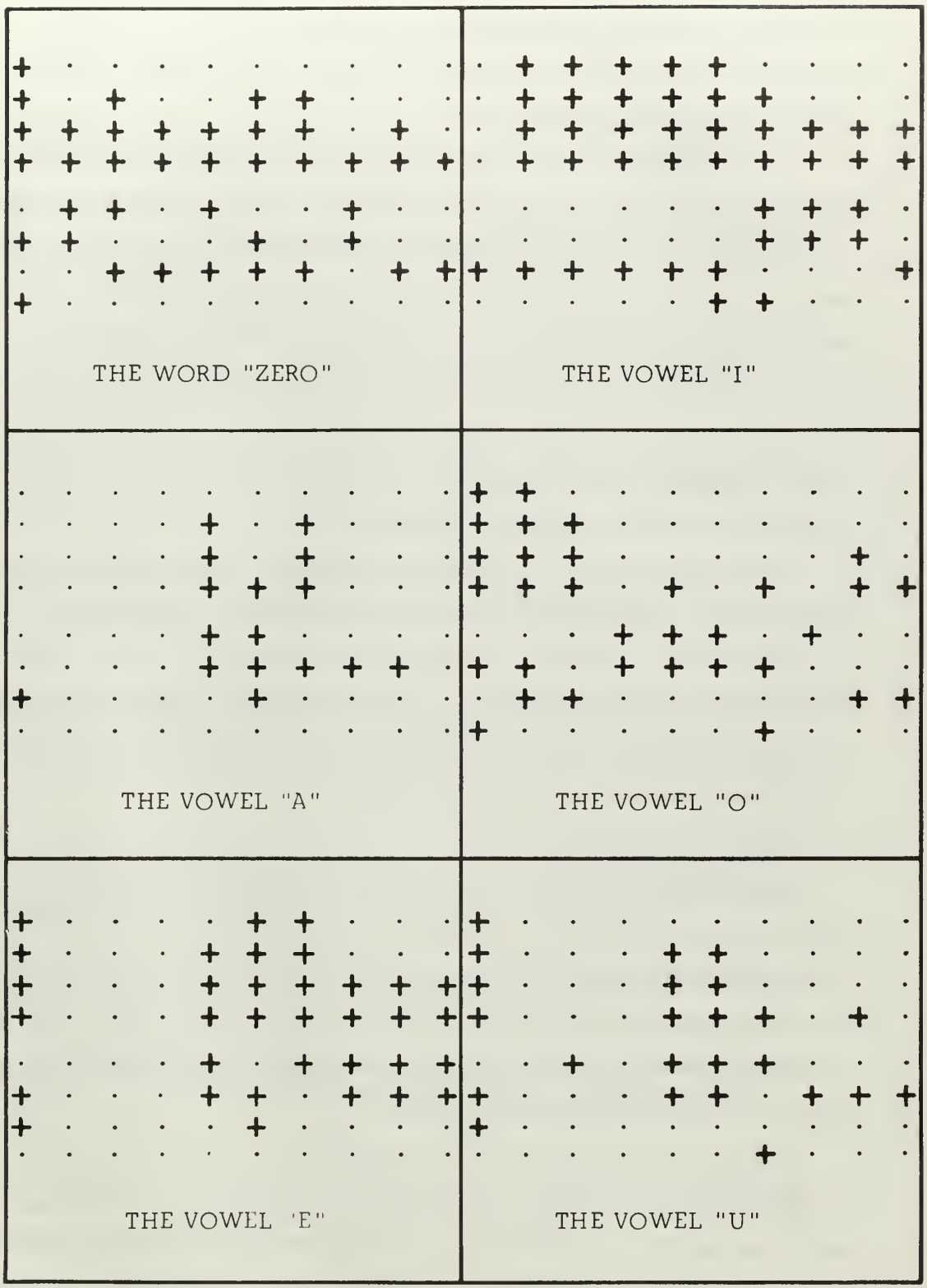


Figure 19. Matrix patterns produced on the prototype equipment. Crosses indicate lamps on, and dots indicate lamps off.

therapy shows that the basic concepts employed herein are valid and feasible. Of major importance is the concept that the inclusion of all possible information in a display of speech for clinical applications is neither necessary nor desirable.

In this regard it is suggested that future efforts be directed toward even greater simplification of the matrix display. Some pre-processing of the input in the form of amplitude range compression seems desirable, and it is evident that wider separation of the amplitude quantization levels would enhance pattern repeatability for variable input conditions. The gain of the preamplifier should be reduced, and due consideration given to the desirability of having channel center frequencies grouped around the frequencies characteristic of the major formants rather than evenly spaced over the voice spectrum.

While the prototype equipment described herein is far from perfect in the eyes of the author, it is felt to be capable of providing much of the information necessary to evaluate the foregoing proposals and others which might occur to persons working in the field. It is hoped that the eventual result will be an inexpensive clinical instrument of significant importance to speech therapists.

16. Acknowledgements.

The author is deeply indebted to Dr. Gerald D. Ewing of the Naval Postgraduate School faculty for first arousing interest in the subject of visible speech, for providing guidance and encouragement throughout, and, most significantly from the point of view of the author, for allowing complete freedom in the development of ideas even though they did not always coincide with his own views.

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# APPENDIX I

## SYSTEM WIRING DIAGRAMS

The main chassis wiring diagram of Figure 21 shows all interconnections between components common to all ten channels and the filter card and processor card connectors for one typical channel. The other nine filter and processor cards are all connected in parallel with those shown, and wire color coding is uniform throughout.

The voltage divider shown connected from the 3.6 volt bus to the Ground bus provides a HI logic level signal to reset the JK Flip Flops in the duration counter circuits. The "Reset" switch simultaneously opens the 24 volt supply line to reset the amplitude detector circuitry.

The power supply wiring diagram shown in Figure 20 is self explanatory. The vertical column of connectors shown on the left are jacks on the front panel of the power supply.

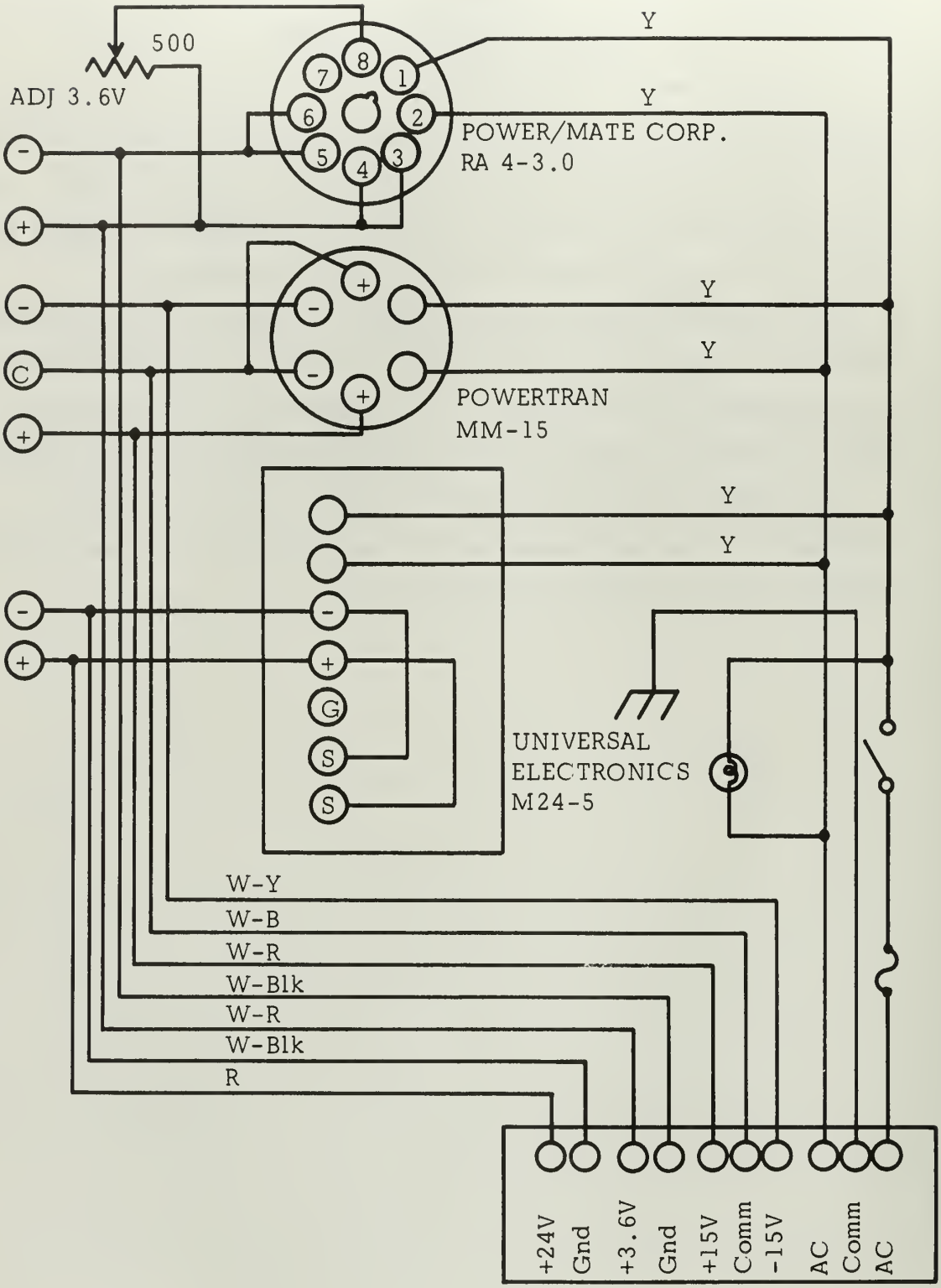



Figure 20. Power Supply Chassis Wiring Diagram.

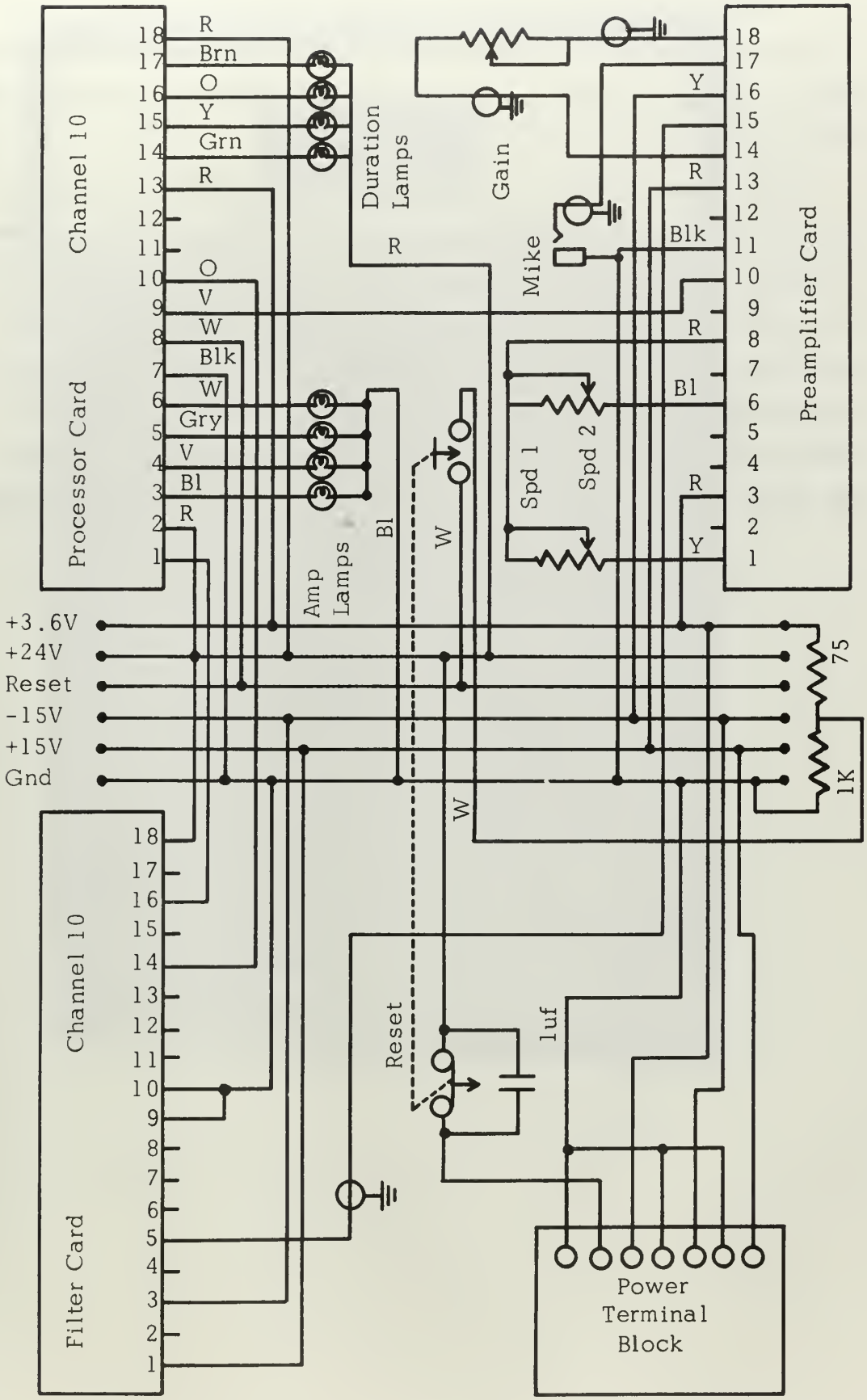



Figure 21. Chassis Wiring Diagram. Connections shown for only one channel of Filter and Processor cards. Connections to other nine channels are identical.

## APPENDIX II

## PHOTOGRAPHIC VIEWS OF PROTOTYPE EQUIPMENT

Various views of the completed prototype equipment are included herein as an aid in understanding the details of fabrication and operation of the system.

The front panel view of Figure 22 shows the matrix display and minimum of operating controls which were basic factors in the concept developed in this paper. Indicator lamps are spaced on one inch centers vertically and one and one-half inch centers horizontally within each sub-matrix, and the two sub-matrices are separated by one and one-half inches. This gives a rectangular display area $7\frac{1}{2}$ inches high by $13\frac{1}{2}$ inches wide which was judged to be an optimal viewing area for an operator seated in a normal position in front of the equipment.

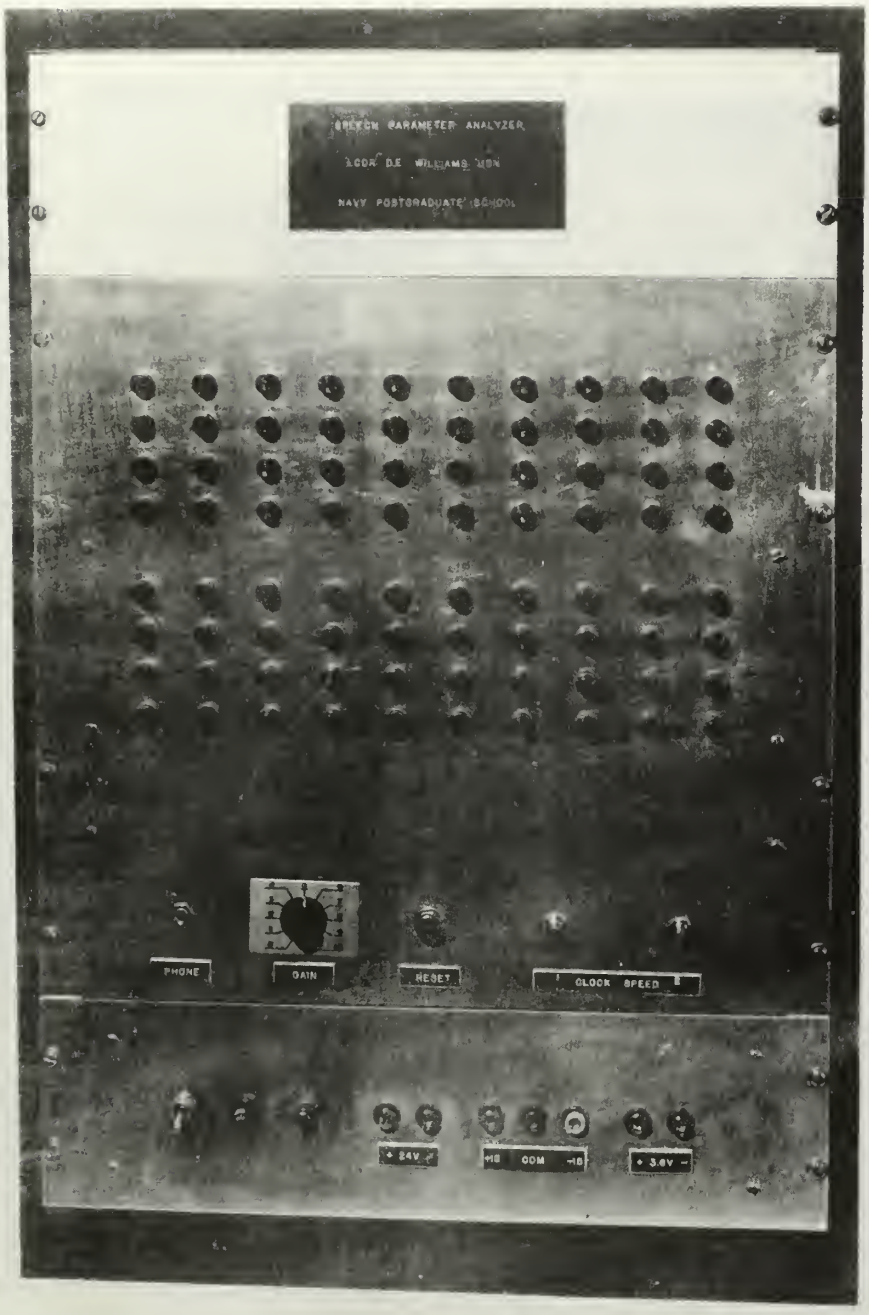



Figure 22. Front View of Prototype Equipment.

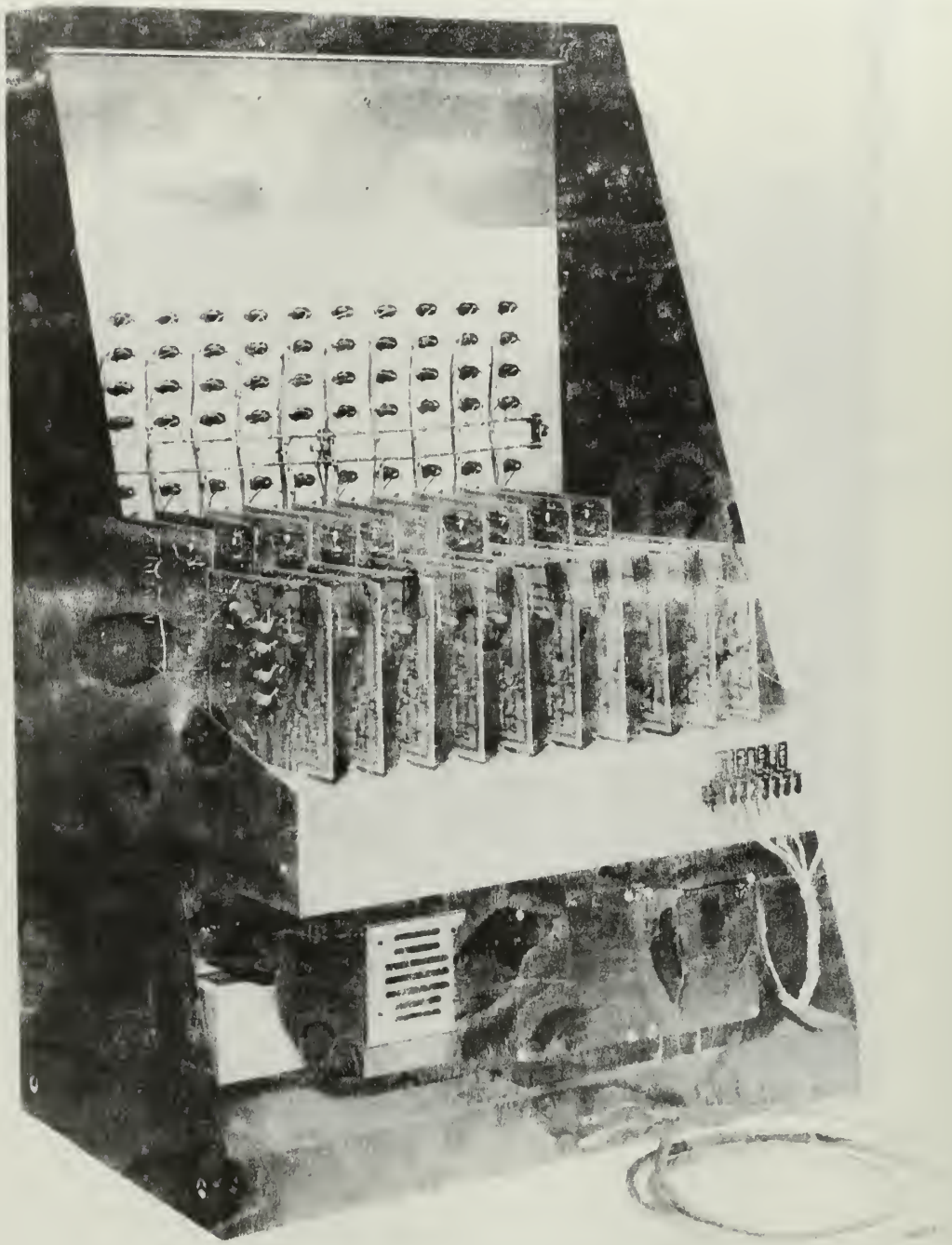
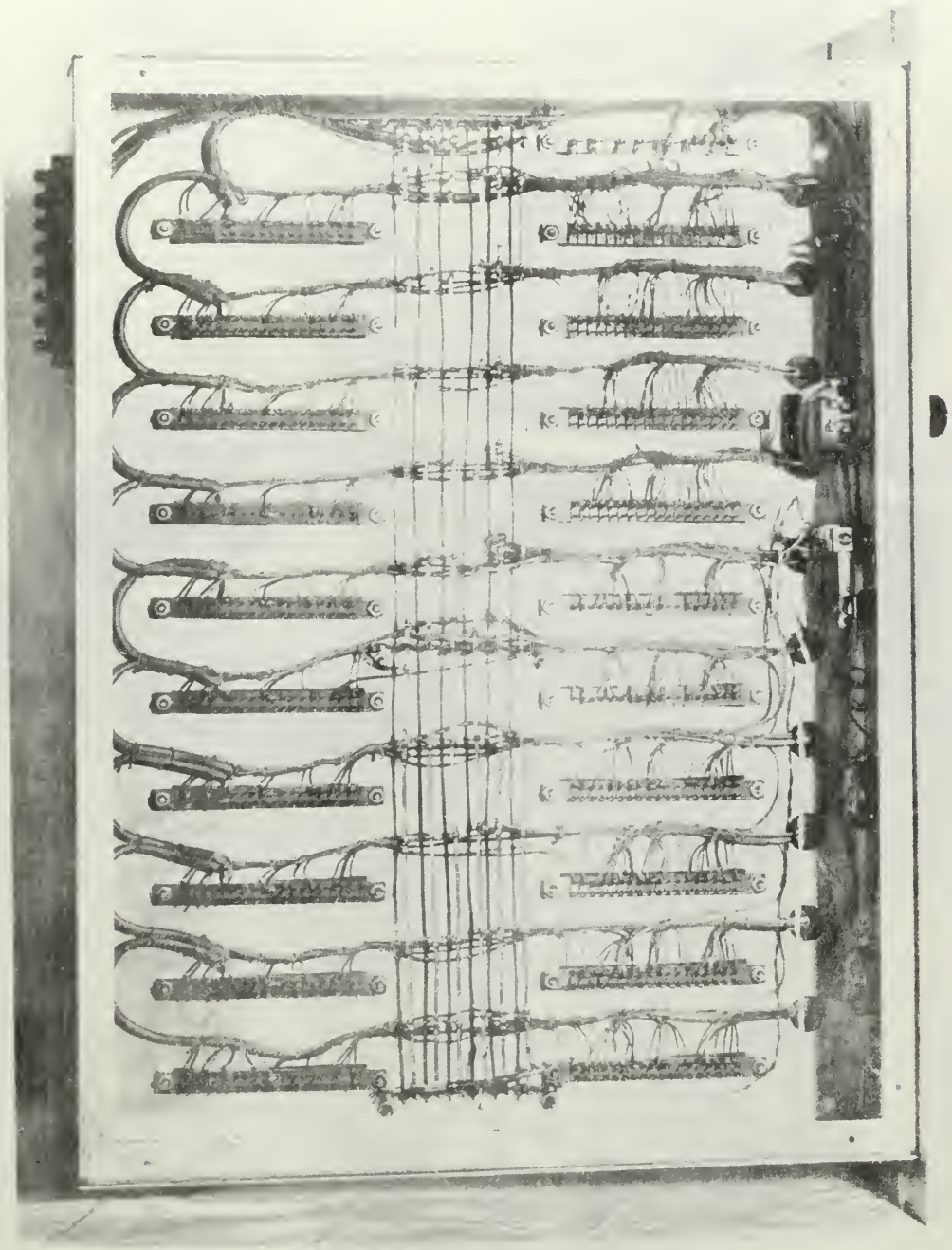


Figure 23. Rear View of Prototype Equipment.



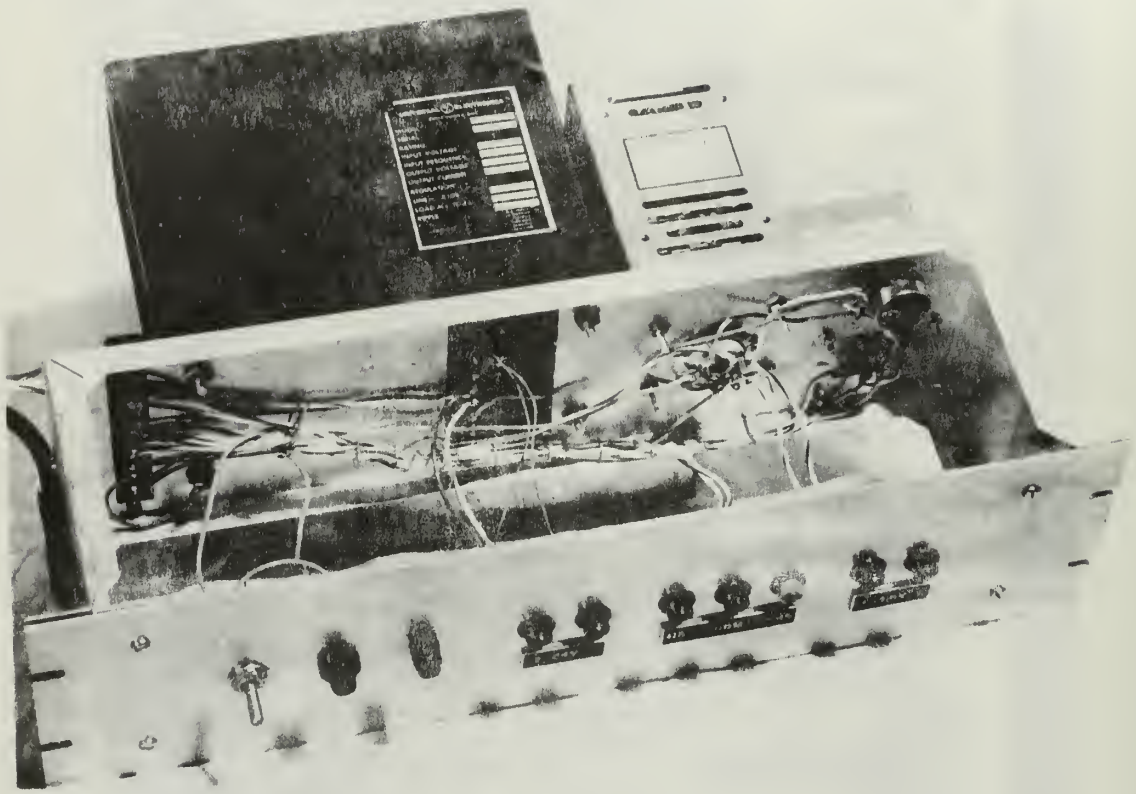


Figure 25. Power Supply Chassis.

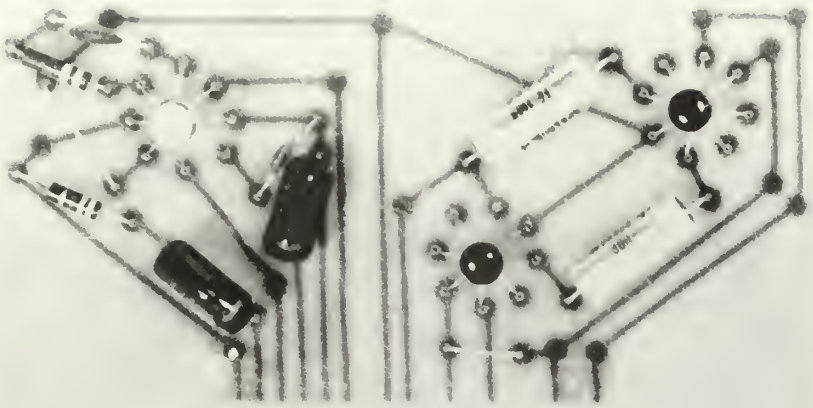


Figure 26. View of Preamplifier card from the component side. Preamplifier circuitry is to the left and clock multivibrator to the right.

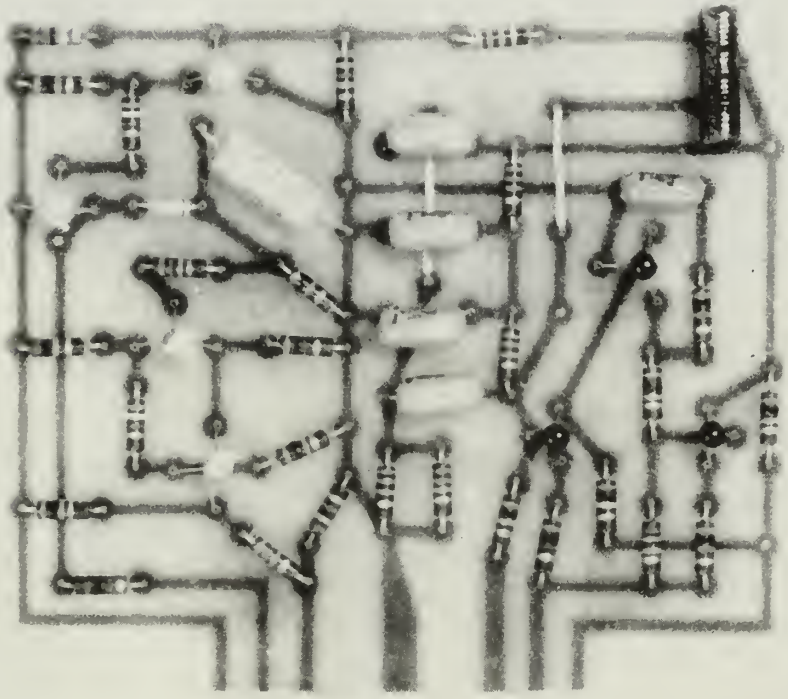


Figure 27. View of the Filter Card from the component side. The active filter is to the right and buffer amplifier, detector and threshold switch to the left.

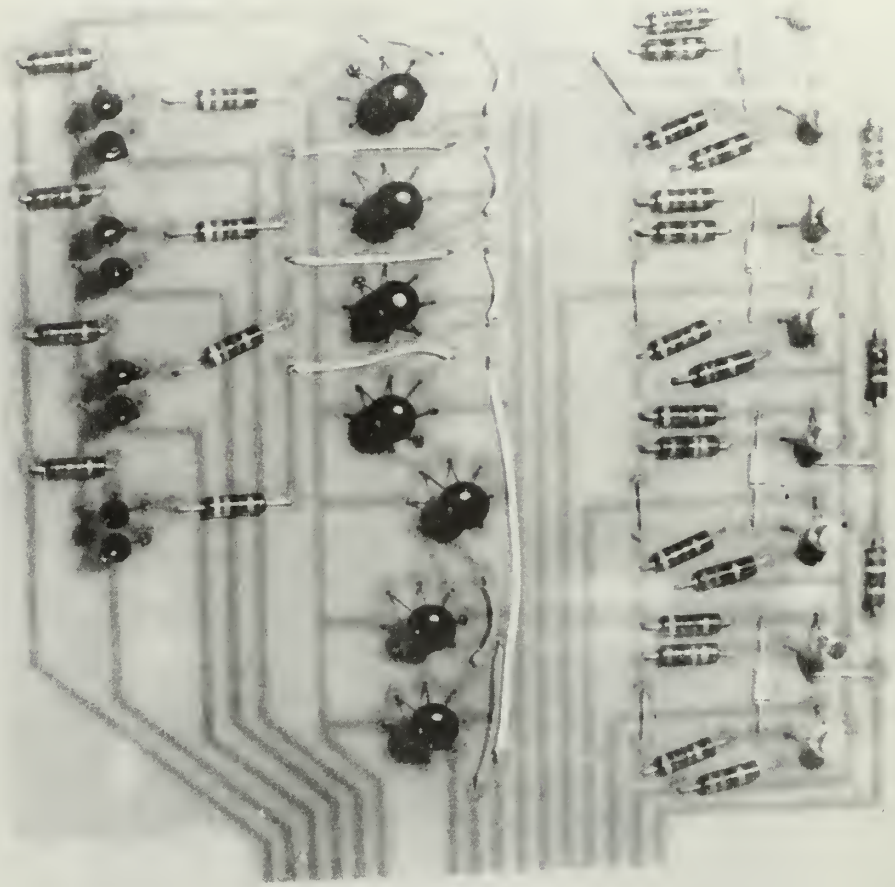


Figure 28. View of Processor Card from the component side. The amplitude detector circuitry is to the right, the duration counter integrated circuits in the center, and the duration lamp drivers to the left.

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13. ABSTRACT

A concept for the visual display of the speech parameters of frequency, amplitude and duration is developed, with emphasis on the use of such a display as an aid in teaching deaf persons to speak correctly. Design criteria for a physical realization of this concept are established and discussed. The complete electronic and mechanical design and fabrication of a prototype speech parameter analyzer is described in detail. Schematic diagrams of all electronic circuitry employed and photographs of the prototype equipment are included. Preliminary performance test results are presented and discussed.

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| Speech Therapy | | | | | | |
| Visible Speech | | | | | | |